

09/674864

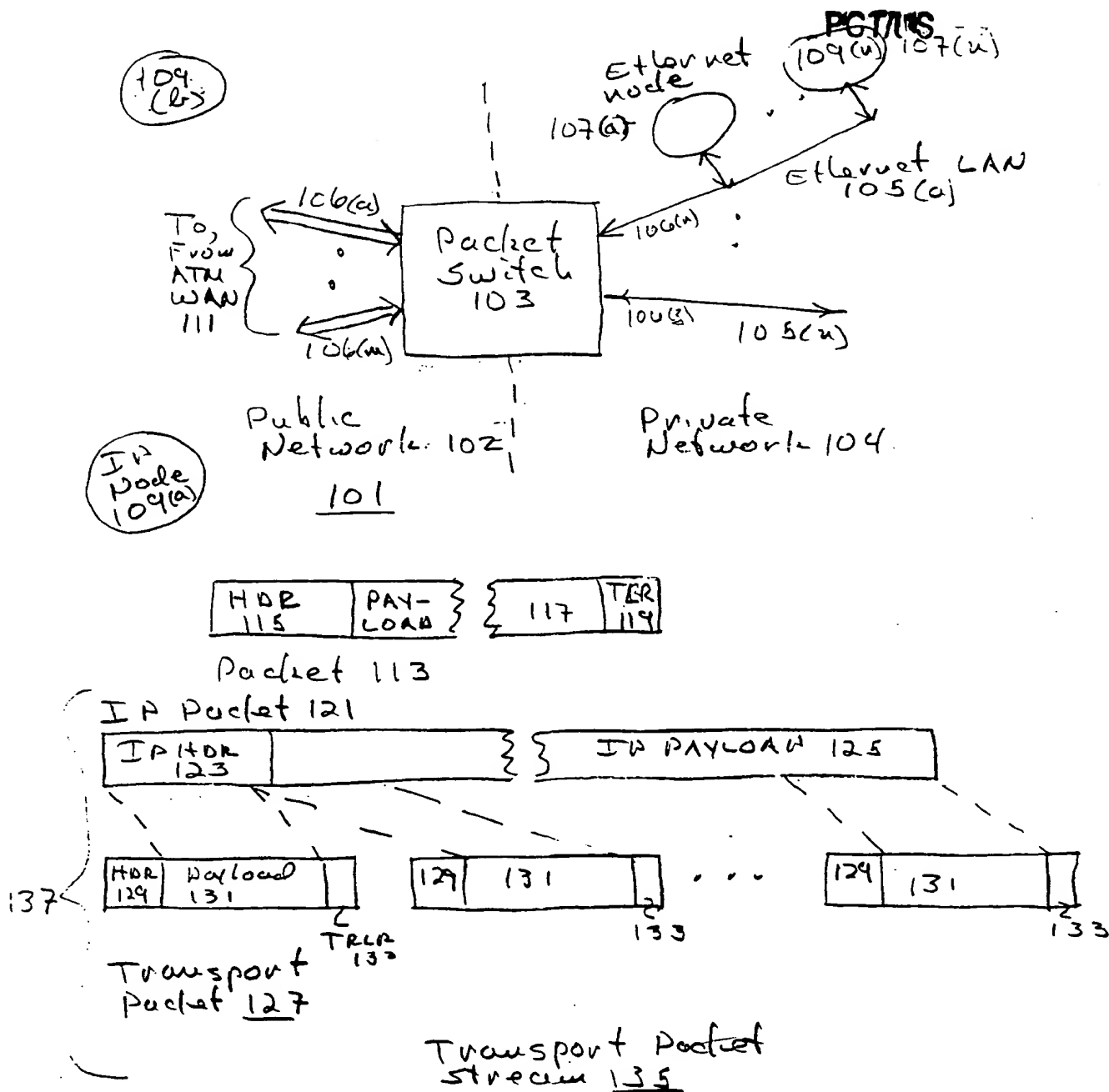
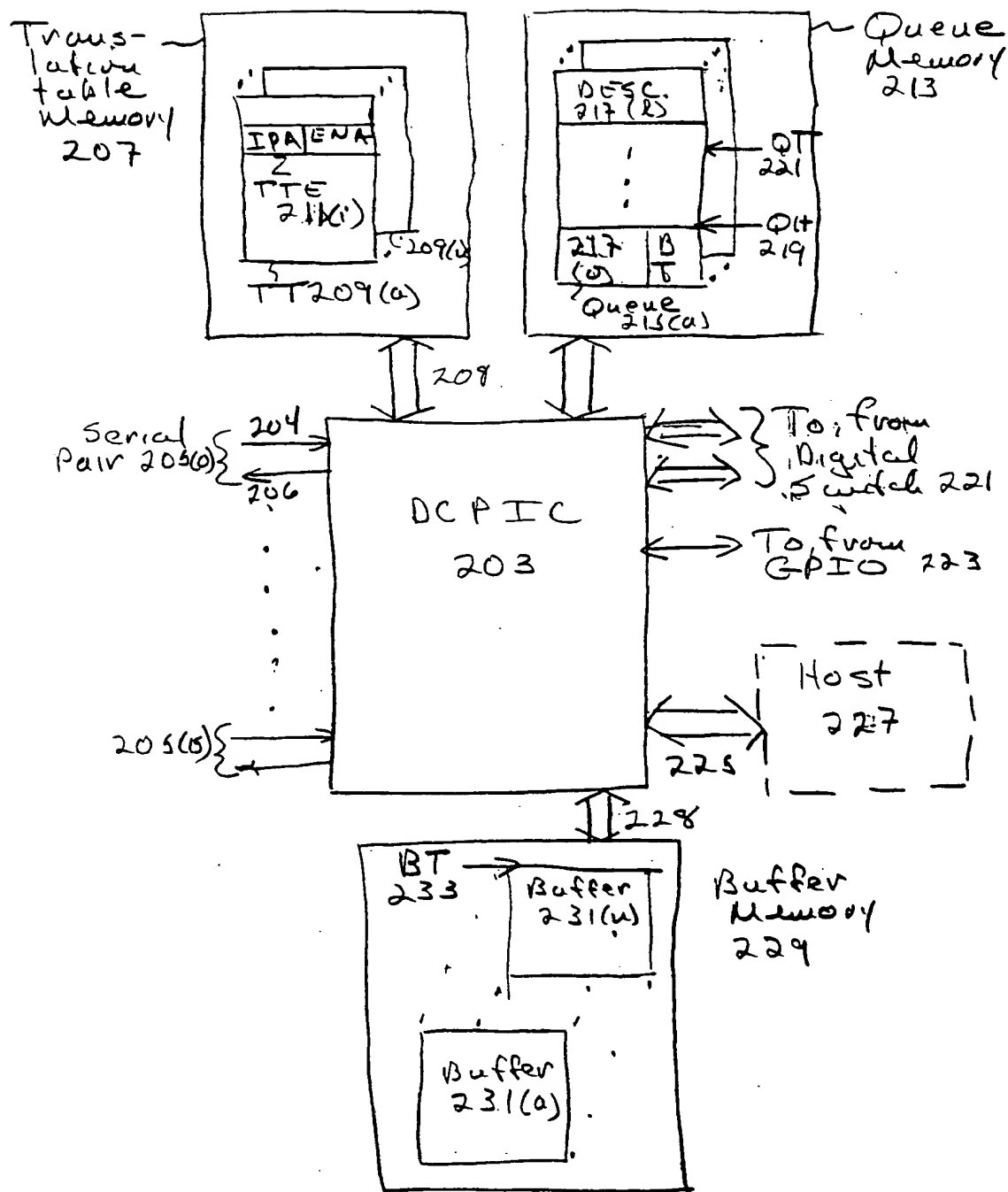


Fig. 1 Prior Art

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201

Fig. 2

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09/674864

Figure 1 DCM Block Diagram

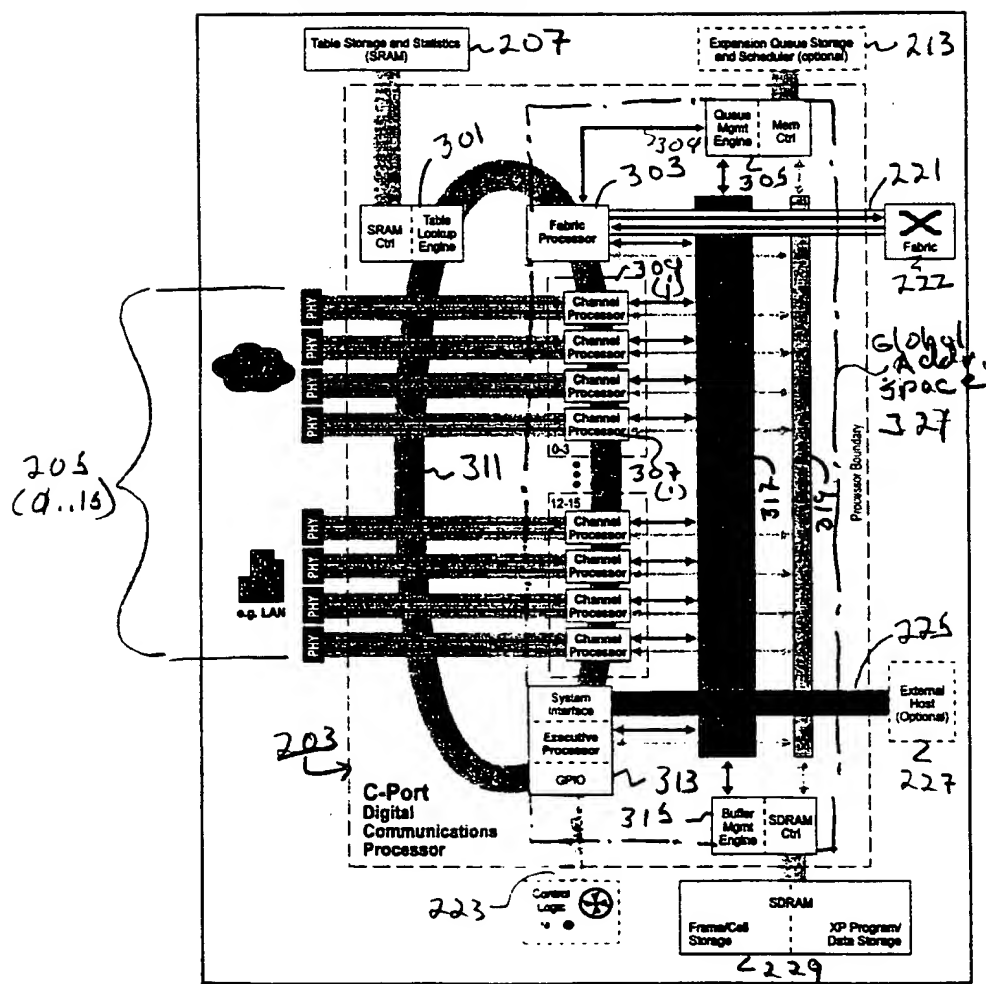


Fig. 3

09/674864

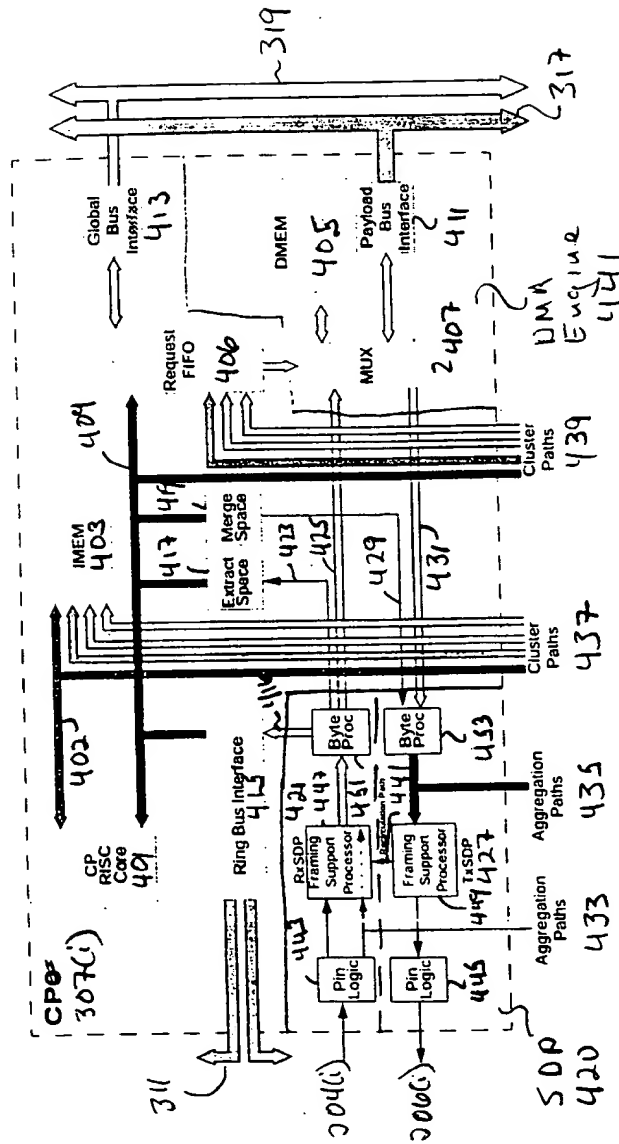
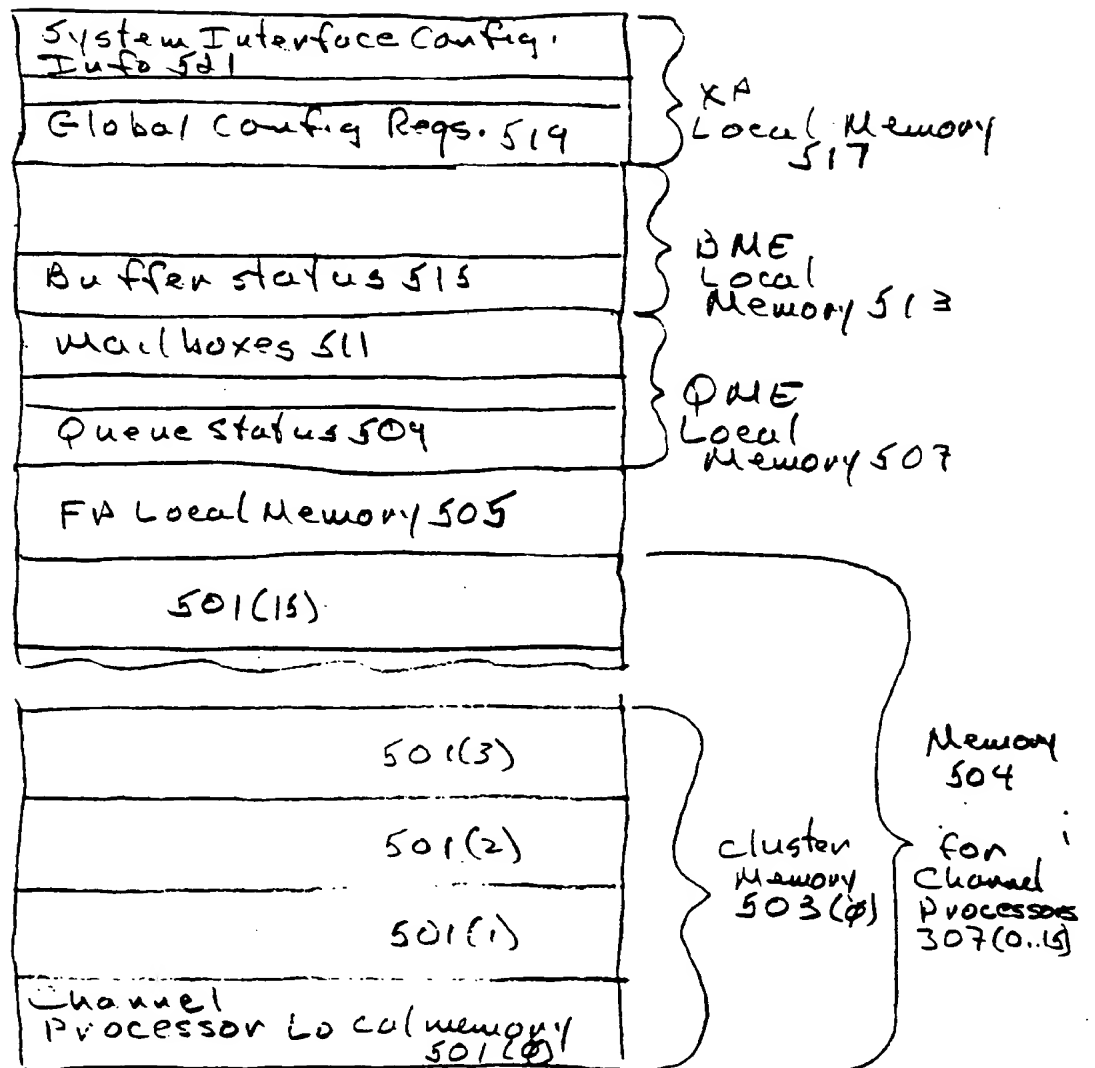


Fig. 4

09/674864



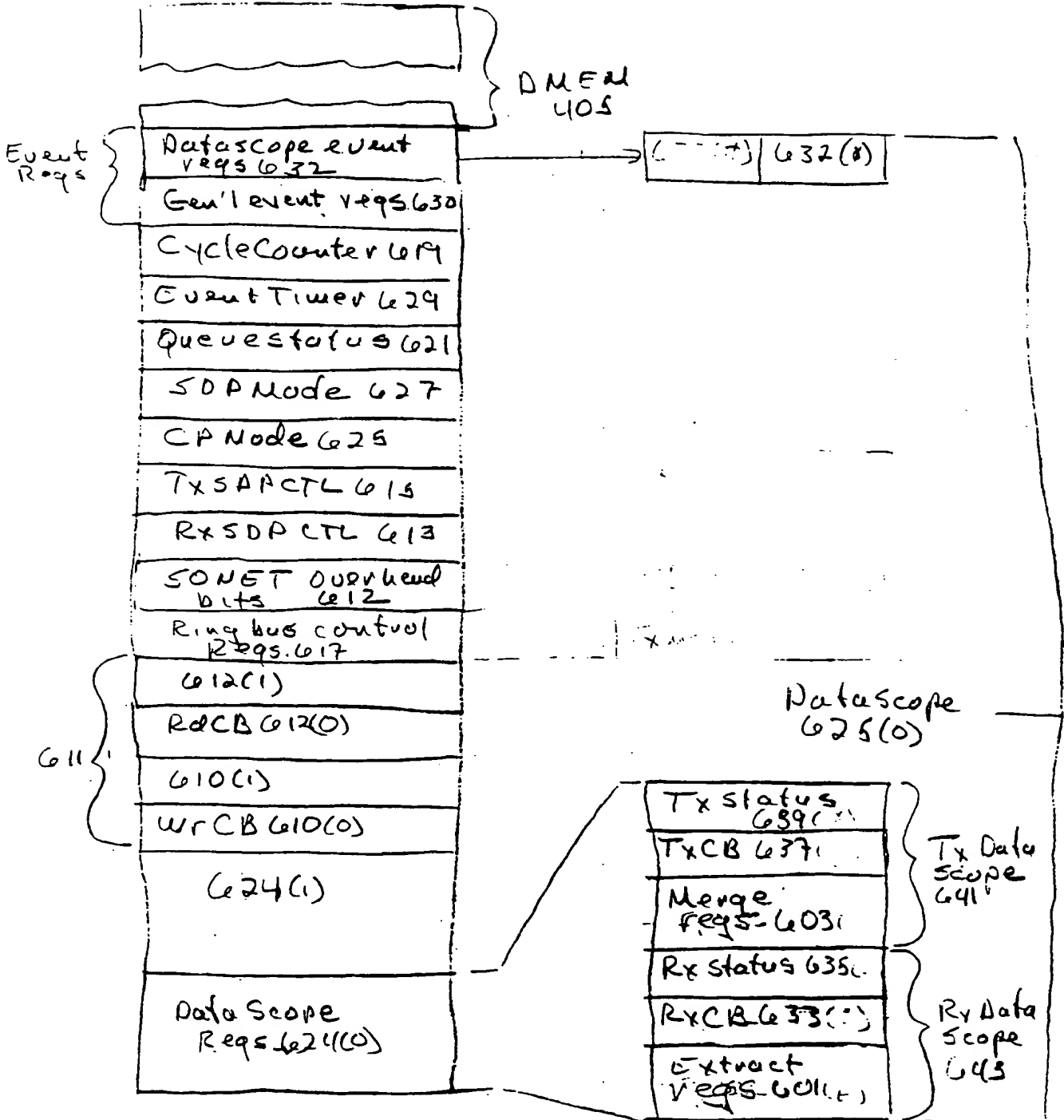
321

Fig. 5

09/674864 "FIG. 5" 1999-04-29

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09674864-033001



11(i)

Fig. 6

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Preliminary Draft

Data Flow in the DCP 1 15

Figure 2—DCP 1 Receive Thread-of-Execution Flowchart

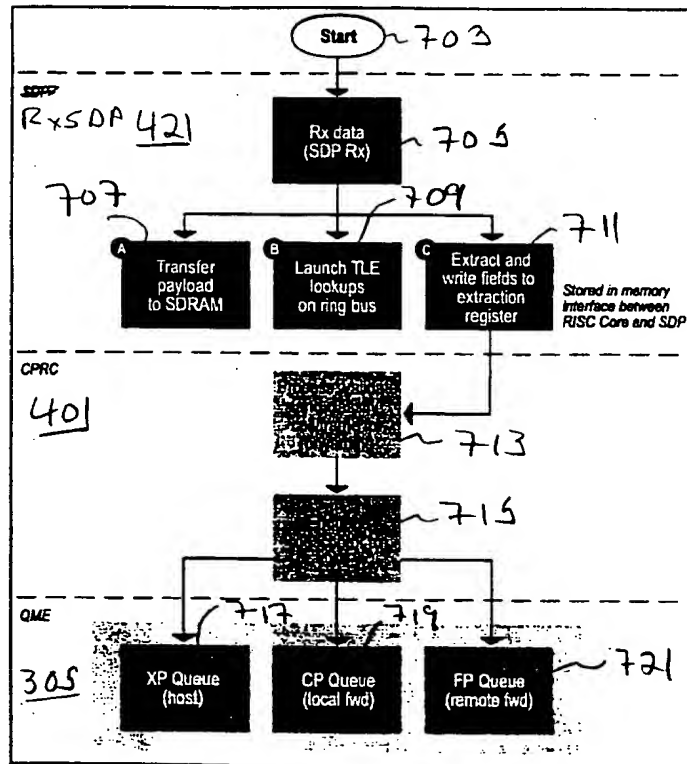


Fig 7

09674864-033001

07/674864

Figure 3 DCP-1 Transmit Execution Thread Flowchart

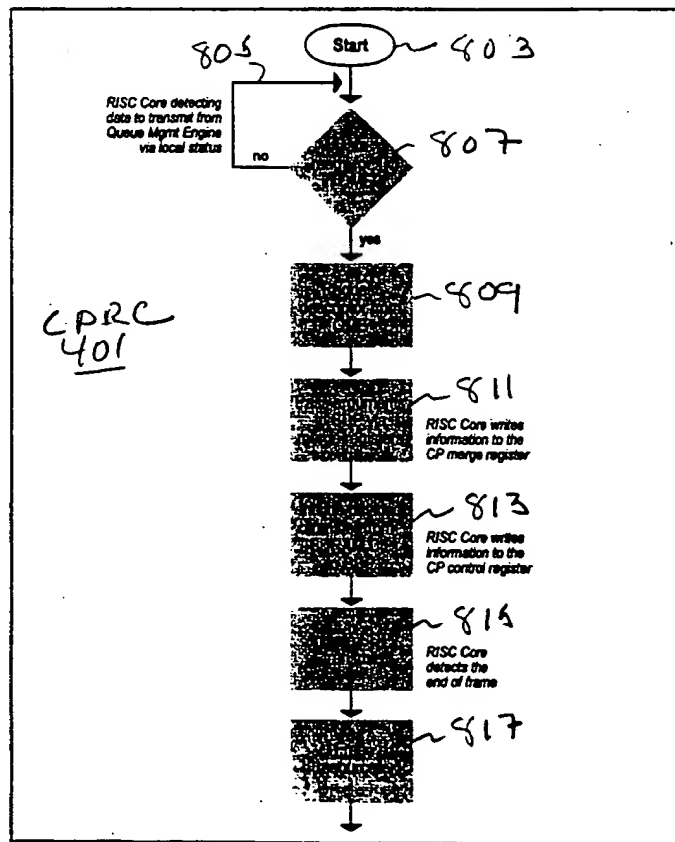


Fig. 8

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OWN 935	LS:LO 937	Busy 941
------------	--------------	-------------

635

BTAG 933			
OFFSET 931			
AV 929	NR 927	ENV 925	OWN 921
SDPST 915	EOP 927	BCTL ST 919	
Length 911			
Buffer Pool No 909			
DMEM OWN ADDR 907			
Tx Recv Addr. 905			
Rx Recv Addr. 903			
DMEM Byte Addr 901			

RxCBCTL 913

633

Fig. 9

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FIG. 10

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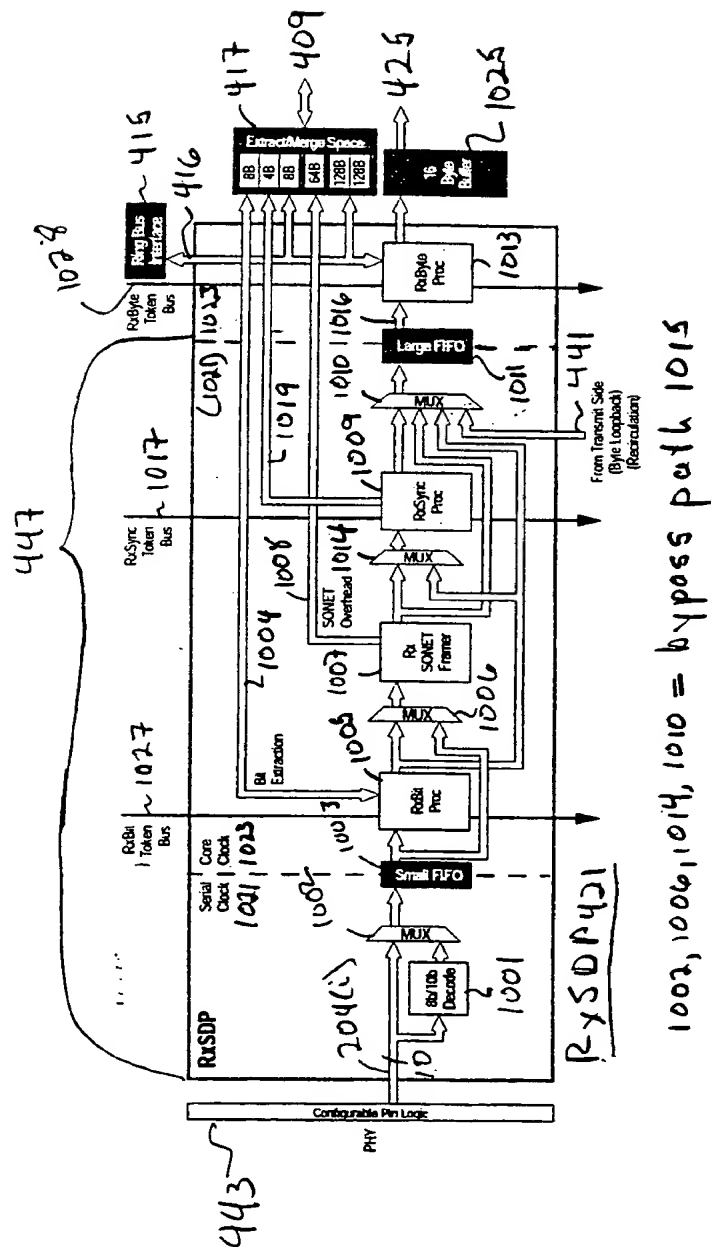
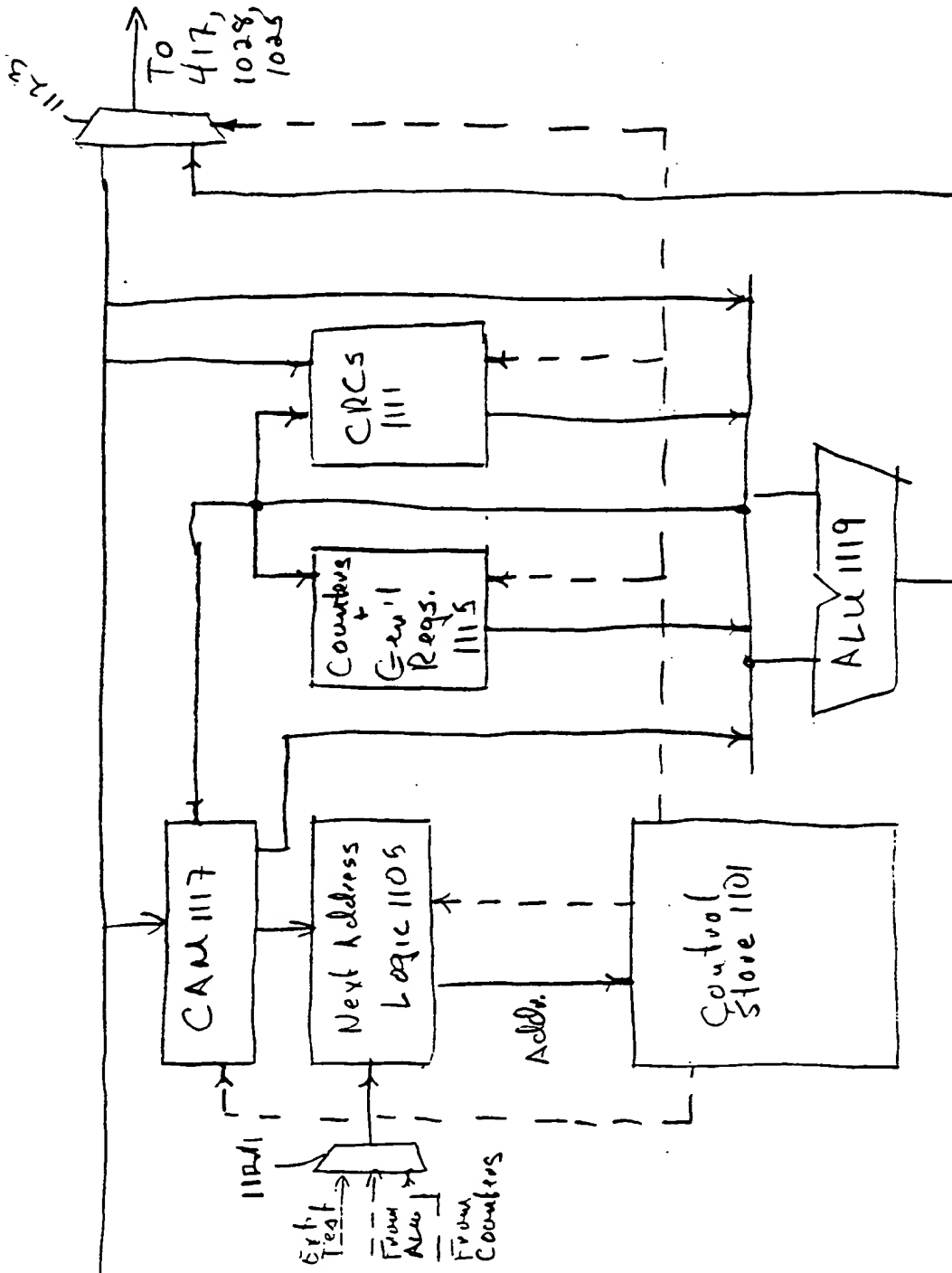


Fig. 10

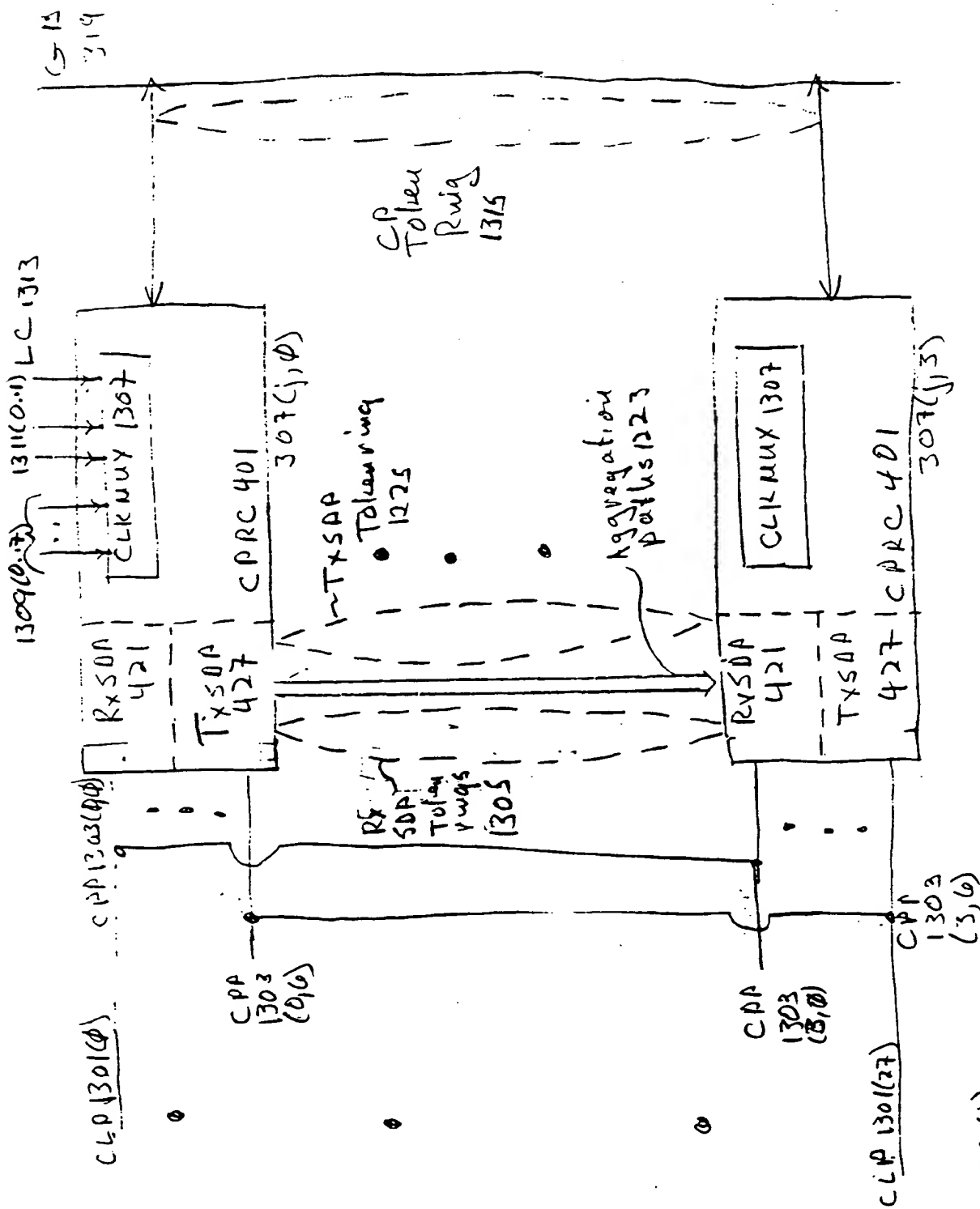
09/67804

FIG. 11



1013

Fig. 11



309(j)

Fig. 13

09/674864

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Preliminary Draft

CP Instruction Memory 29

CP Instruction Memory

Each channel shares access to a 16kB IMEM among a cluster of four adjacent CPs as shown in Figure 7. The IMEM is configured as four sub-arrays, with each CP in the cluster given access to the arrays, one per cycle, in fixed round-robin order. With this simple interleaved scheme, the four adjacent RCs can access this memory at nearly full bandwidth.

When adjacent channels are configured to handle similar communication protocols, the large shared memory can contain both channel-specific code and cluster-shared code such as exception routines.

At initialization time, the 16kB array can be divided so that each CP gets a dedicated 4kB sub-array. This array allocation removes all CP contention for IMEM (but also removes the opportunity to share code among CPs). The memory configuration options result in roughly the CPRC performance shown in Table 6-1 for non-blocking code. The *optimized* column means that the compiler has placed code such that the branch target address bits <3:2> equal the branch fall through address bits <3:2>. CPRC instruction references outside of the shared local memory space are not supported.

Table 3 Channel RISC Core Instruction Execution Efficiency

IPC	IPC optimized	CP IMEM configuration
.85	.90	4 CPs sharing 16kB
.95	N/A	each CP accessing a single 4kB sub-array

Figure 7 Local and Shared Memory in a Channel Cluster

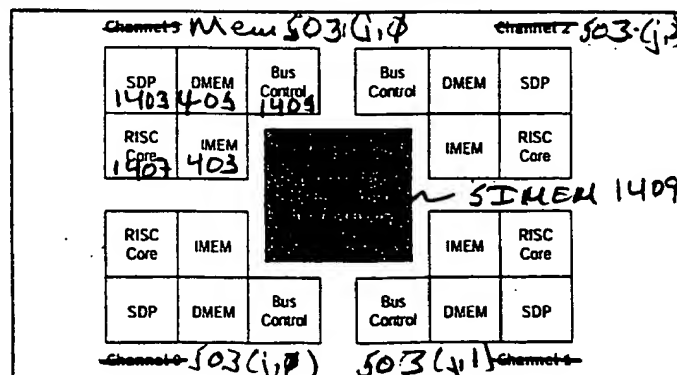


Fig. 14

509

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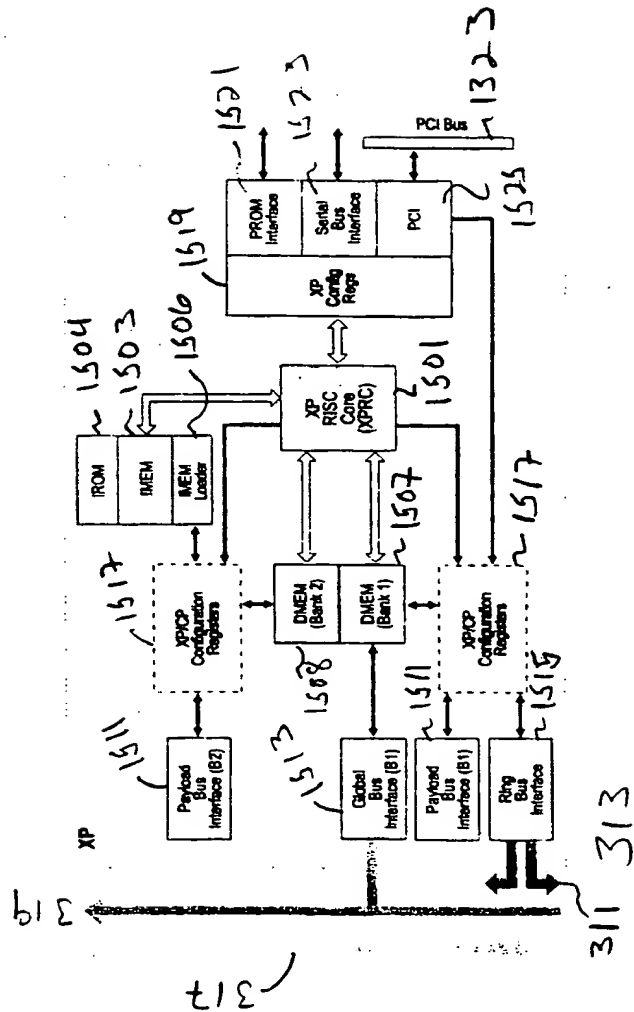


Fig. 15

09/67488

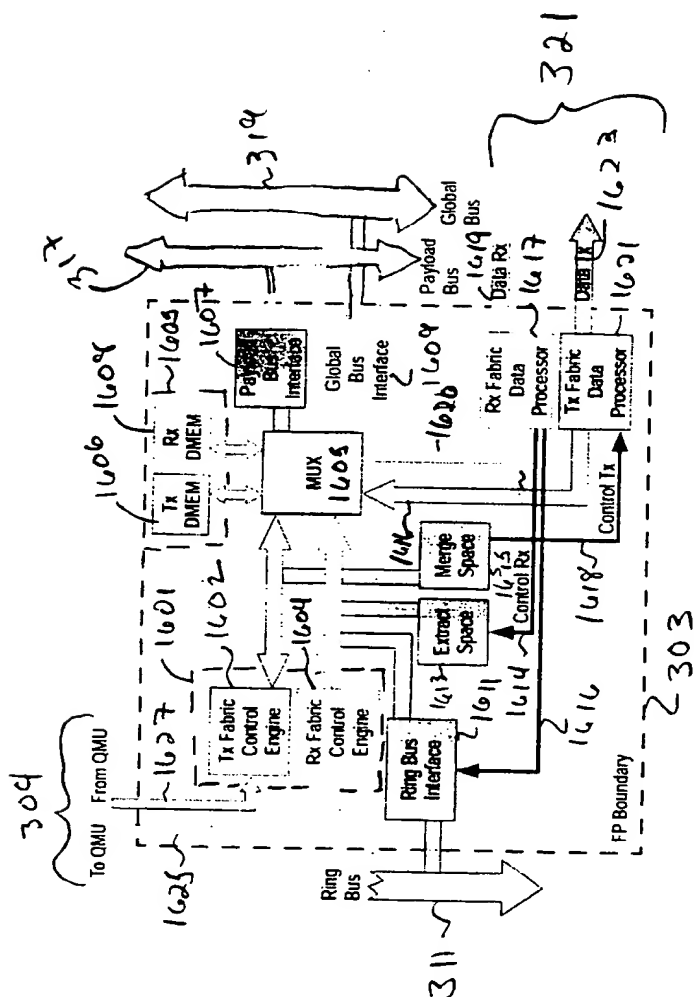
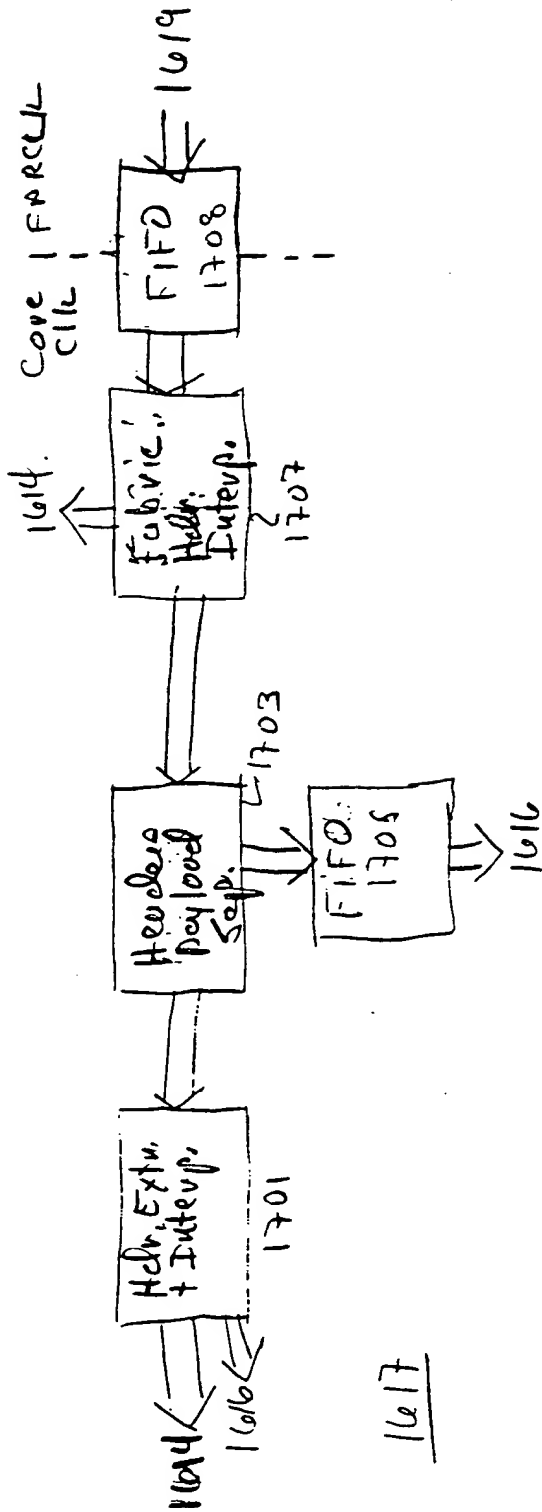
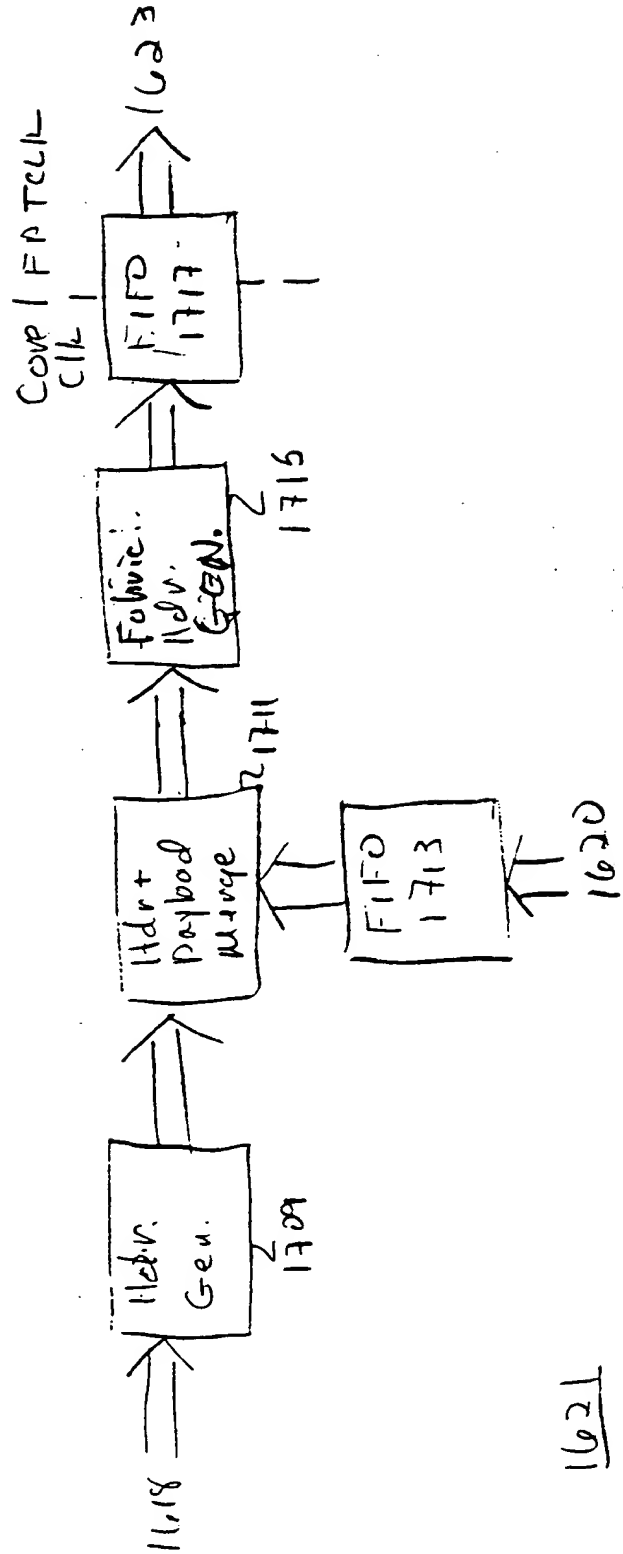


Fig. 16

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1617



1621

Fig. 17

09/674804

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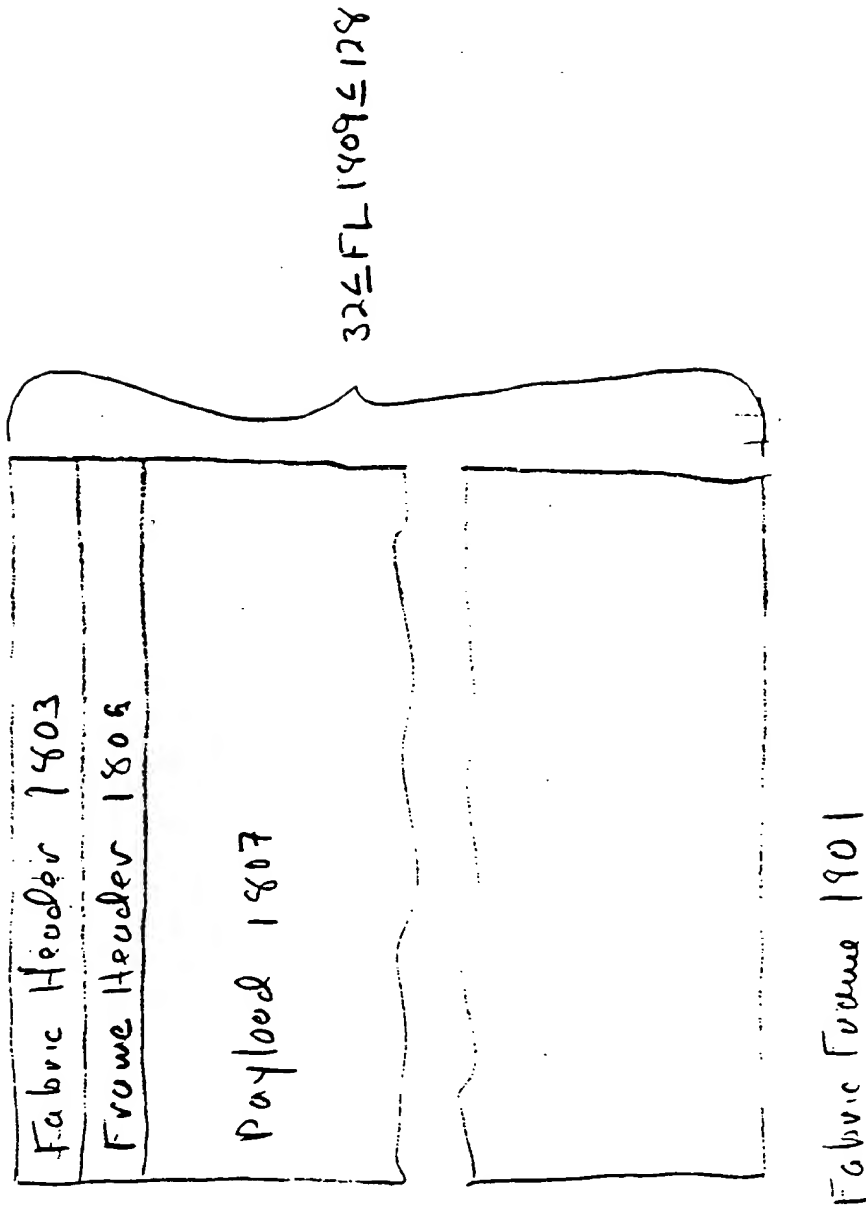
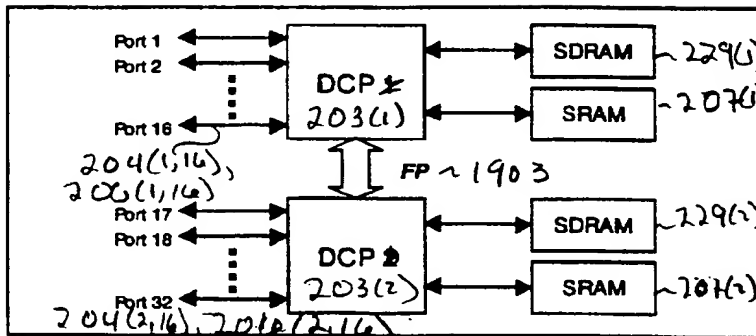


Fig. 18

09/674864

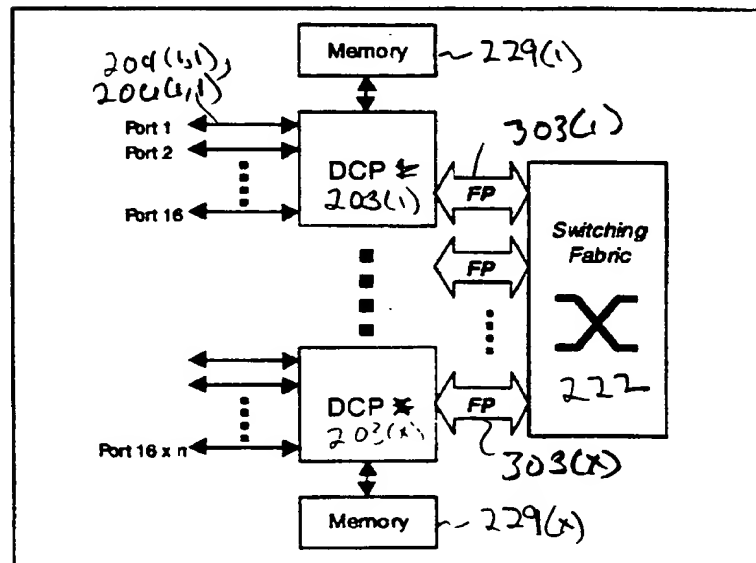
Figure 12 Two DCP-1 Application



1905

When more than two DCP-1s are required in a system, a switching fabric is utilized. The switching solution has two or more FP-type ports and provides a mechanism for switching cell- or packet-based data from one DCP-1 to another. An homogenous, multi-DCP-1 application is shown in Figure 13.

Figure 13 Multiple DCPs with Switching Fabric



1901

Fig. 19

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09/67486d

Figure 14 Heterogeneous DCP-1 Switching Application

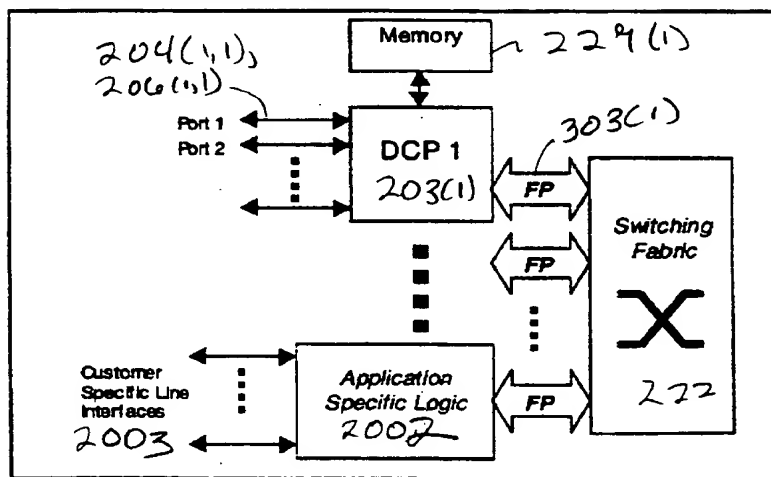


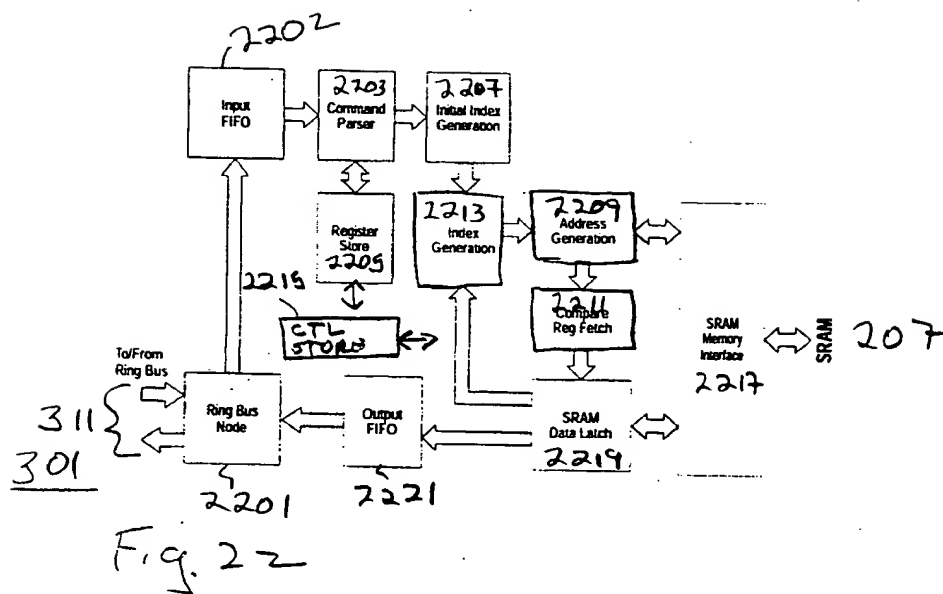
Fig. 20

09/67486d

The diagram illustrates a data structure with three main tables and several associated data blocks and pointers:

- TP 2101(6)**: The top table, containing a block labeled **Alg. Desc. 2123**. Above this block, the text **Alg. # 2123** and **2124** are written. Below the block, the text **VTNS 2127** and **Alg. Spec. 2129** are written.
- TP 2101(4)**: The middle table, containing a block labeled **Link Table 2107 (2106)**. To the right of this block, a box labeled **LTE 2111** is shown, with an arrow pointing from the table to it. Below the box, the text **LIX 2109** is written.
- TP 2101(7)**: The bottom table, containing a block labeled **Data Table 2117**. To the right of this block, a box labeled **CTE Info 2113** and **Link Info 2115** is shown, with an arrow pointing from the table to it. Below the box, the text **2111** is written.
- Other Elements**:
 - A box labeled **KEY 2120** and **Data 2121** is shown at the bottom right, with an arrow pointing from the table to it. Below this box, the text **2119** is written.
 - A box labeled **WTE 2119** is shown below the **Data Table 2117** block, with an arrow pointing from the table to it. Below this box, the text **207** is written.
 - A box labeled **209** is shown to the right of the **Link Table 2107** block.

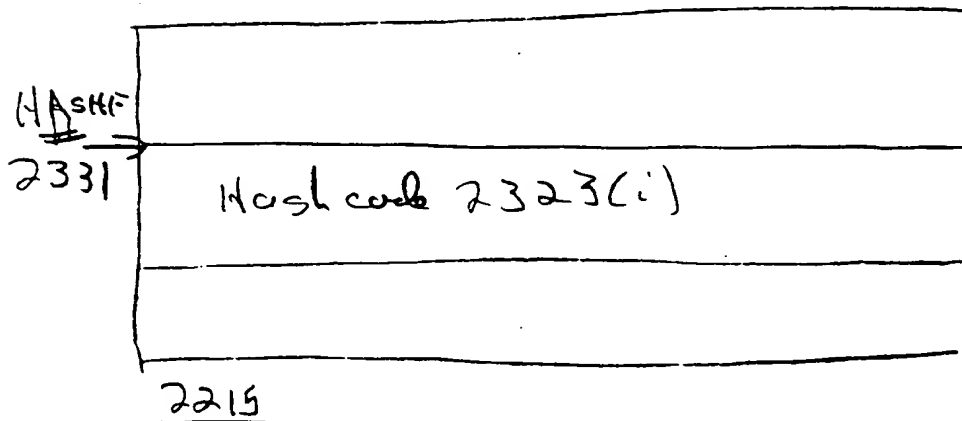
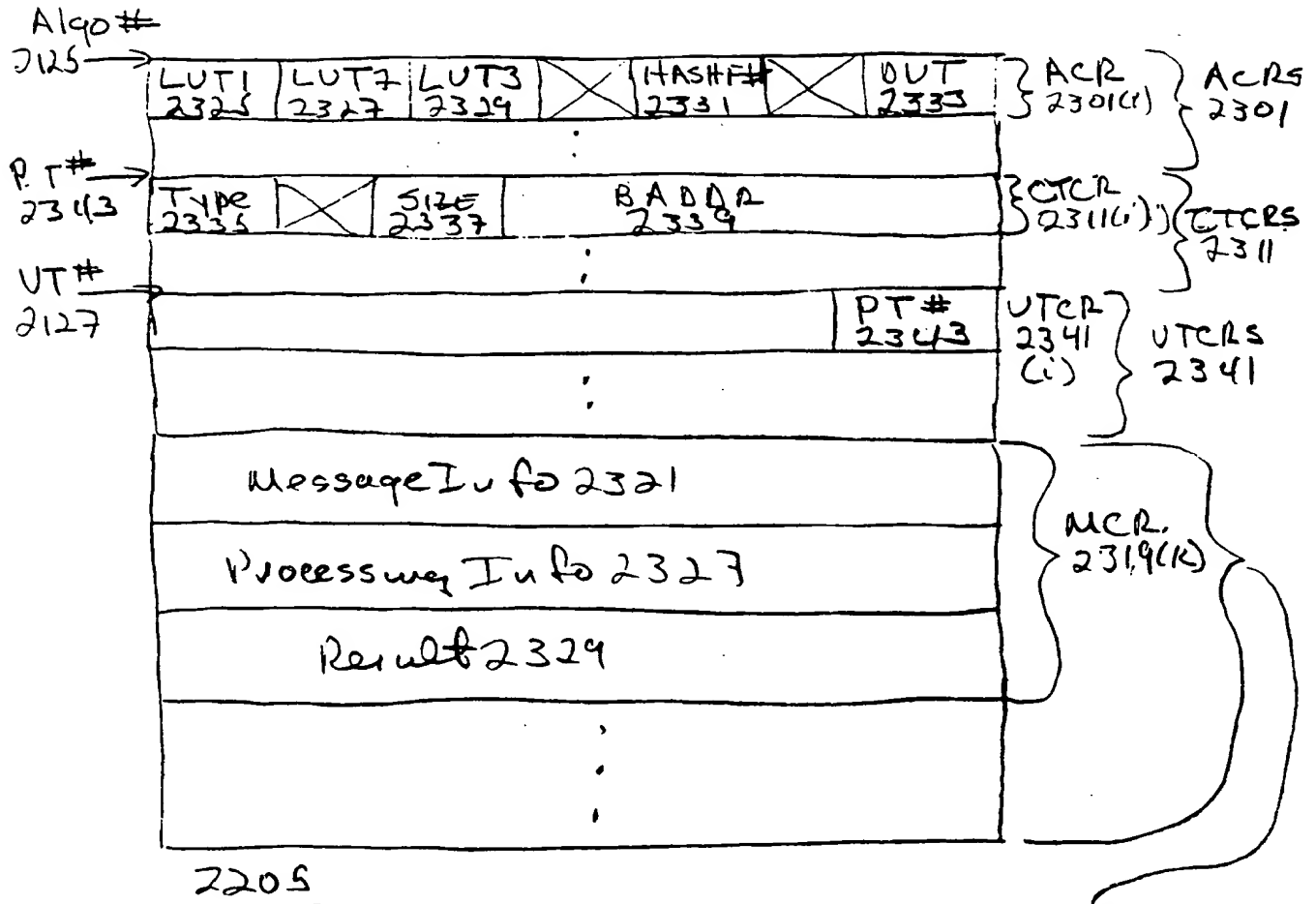
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FIG. 23



Message
Context
Registers
2319

07/674864

Command	Command ID	Return Data	Description
2421 { Write(vtable#, index, mask, data, offset, length)	0x2	None	Write data into a virtual table at index. ~2401
Read(vtable#, index, offset, length)	0x3	Data	Reads data from a virtual table. ~2403
Find(alg#, key)	0x6	Physical Table, Index, Error	Finds a key using alg#. Sets Ring Bus Error Flag if key is not found. ~2405
2423 { FindW(alg#, key, data, offset, length)	0x4	Pass/Fail, Index, Error	Writes data into a table using a key. Sets Ring Bus Error Flag if the key is not found. ~2407
FindR(alg#, key, data, offset, length)	0x5	Pass/Fail, Index, data	Reads length dwords of data from a vtable# using a key at offset dwords. Sets Ring Bus Error Flag if the key is not found. ~2409
2425 { XOR(vtable#, Index, data/pcrc, offset, mask, crc, last)	0x1	None or CRC in CRC mode.	XORs up to a 32 bit value to offset. Only masks of up to four consecutive bytes are valid. A special mode exists for CRC calculations. ~2411
Add(vtable#, index, data, offset, mask)	0x7	None	Adds up to a 32-bit value to offset. Only masks of up to four consecutive bytes are valid. ~2413
2427 { WriteReg(reg_addr, data)	0x0,0x10	None	Write data to TLE register at reg_addr. ~2415
ReadReg(reg_addr, data)	0x0,0x11	Data	Read data from TLE register at reg_addr. ~2417
Echo(data)	0x0,0x04	Data	Returns data from TLE. For test purposes. ~2419
Nop()	0x0,0x05	None	Inserts a NOP into the TLE pipe. ~2420

Fig. 24

T00000-1934250

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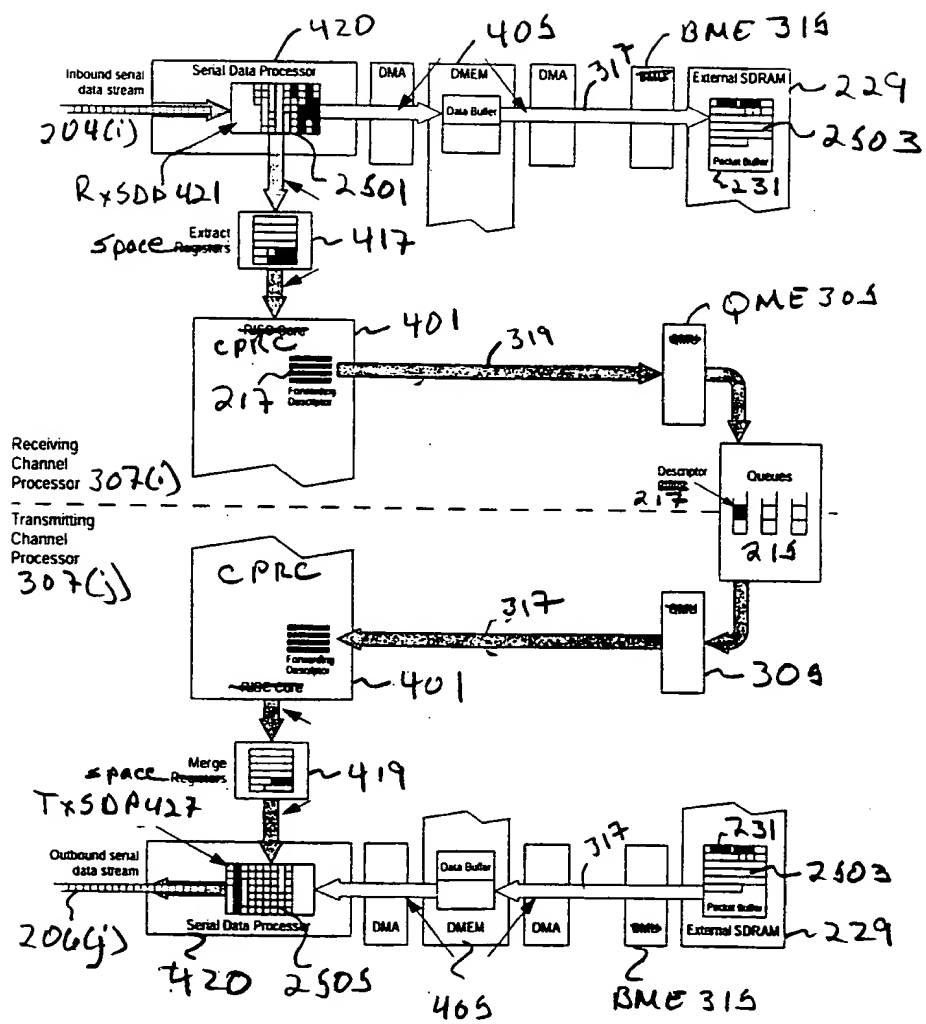


Fig. 25

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09/674864

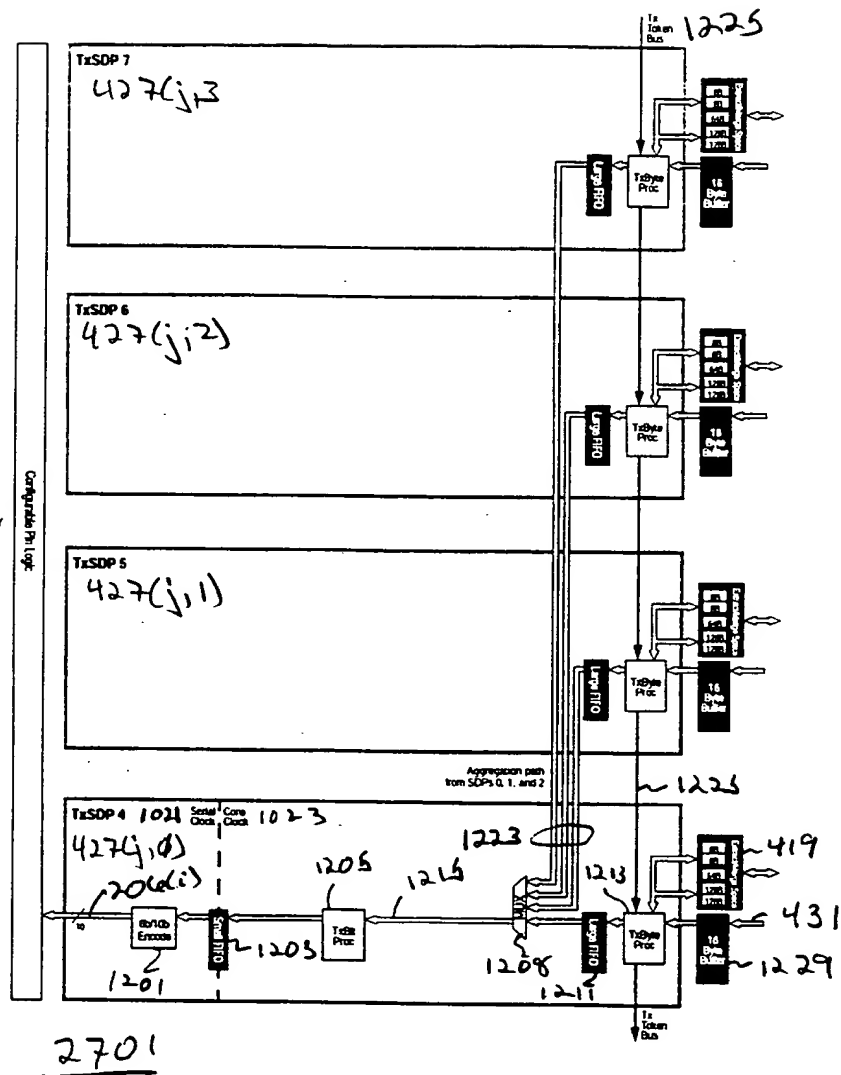
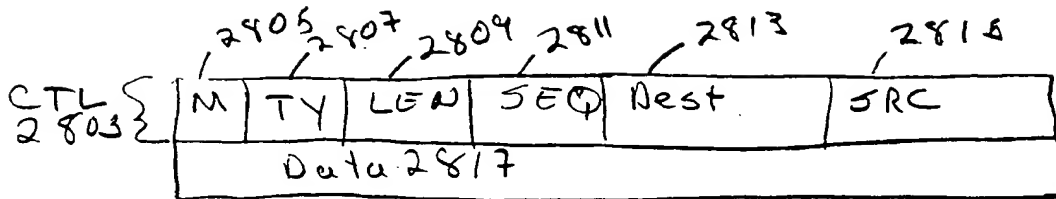


Fig. 27

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Ring bus message 2801

Fig. 28

09674864-03001

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09674864-03001

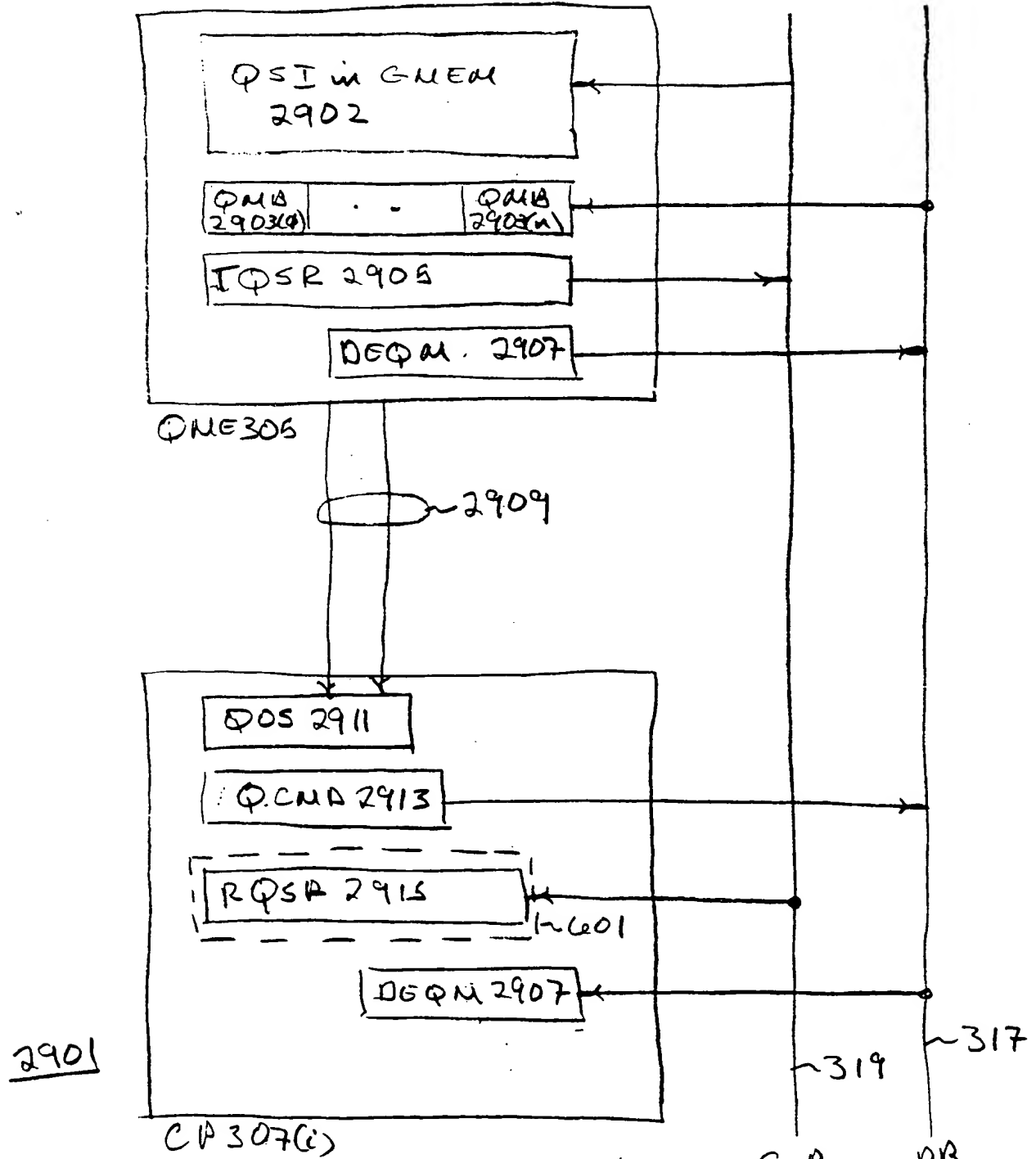
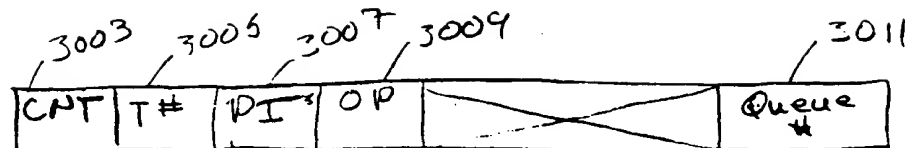


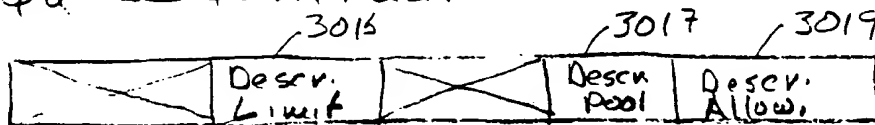
Fig. 29

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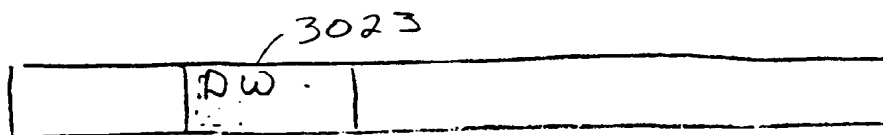
09/674864



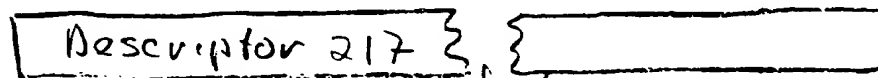
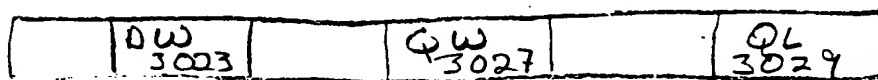
Queue Inst. Addr. 3001



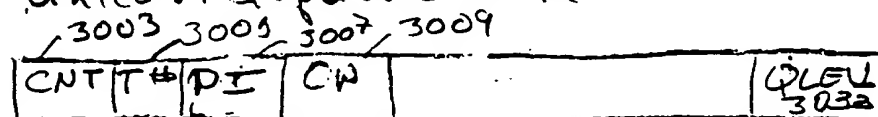
Configure Queue Write Data 3013



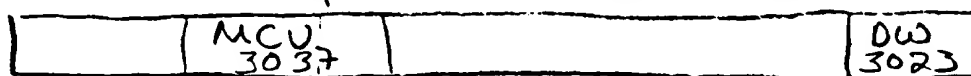
Unicast Enqueue Data



Unicast dequeue data



Multicast Enqueue Inst. Addr. 3031



Multicast Enqueue Data
30/47

2913

Fig. 30

FIG. 30

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FIG. 31

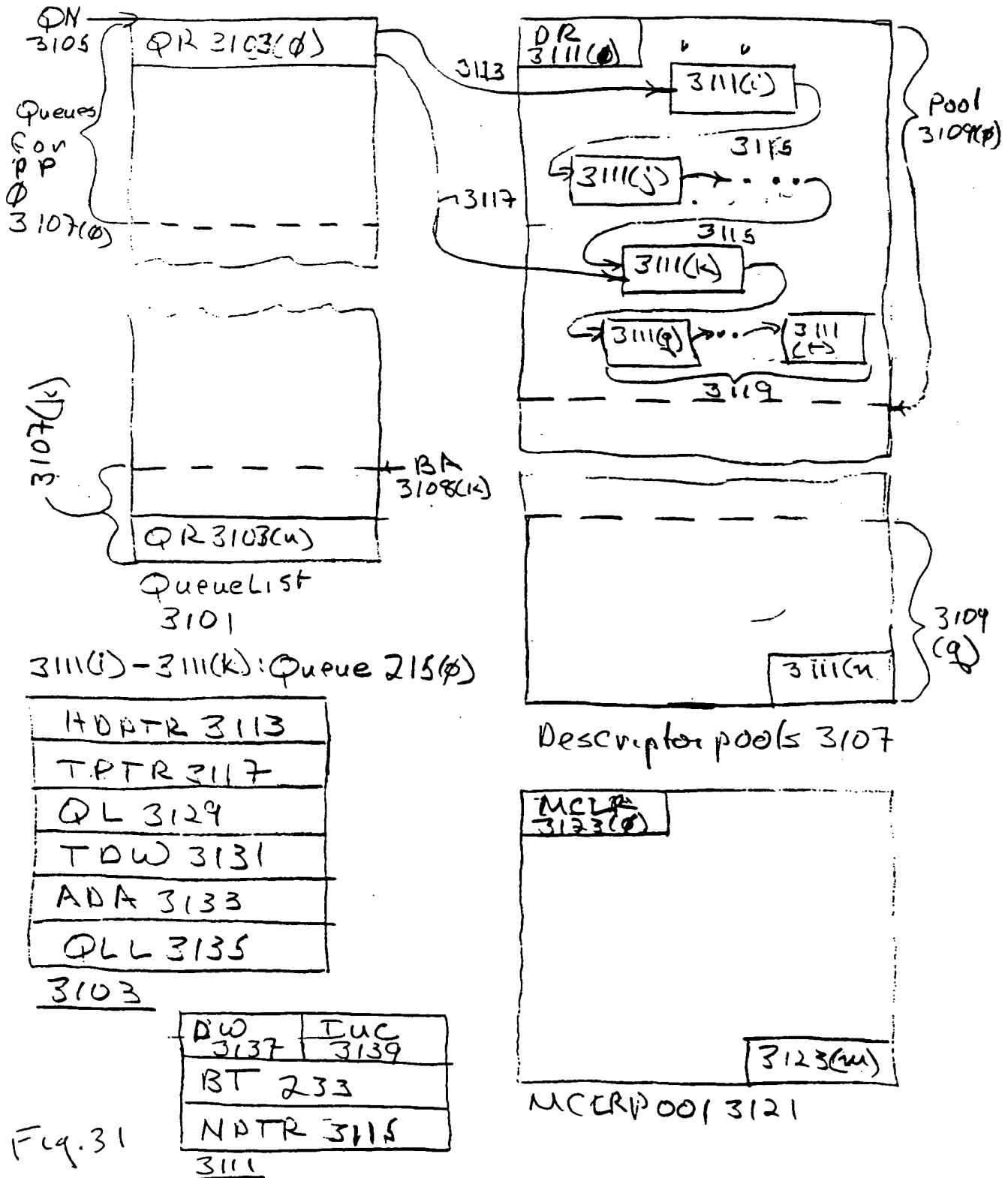
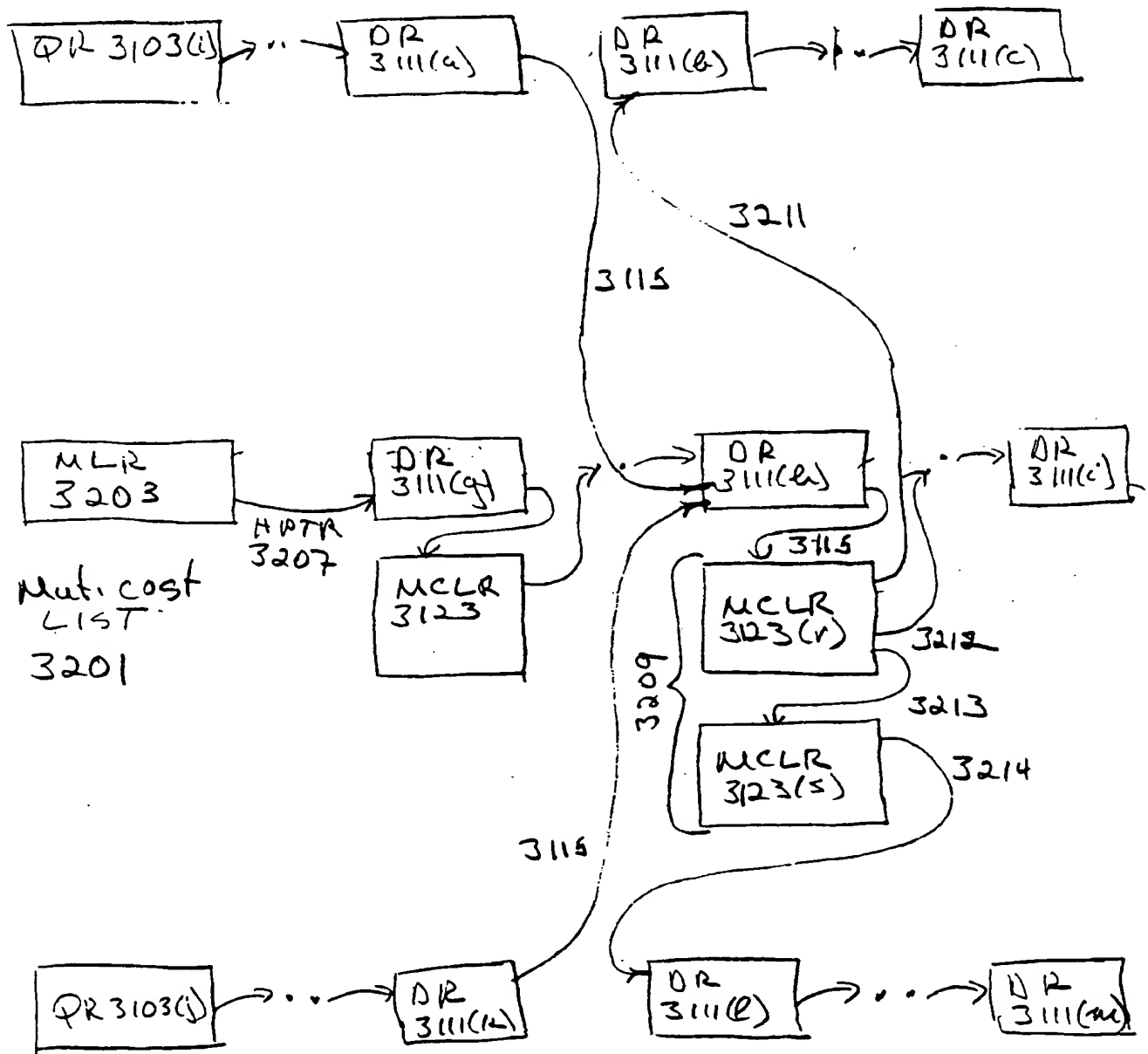


Fig. 31

09/674864

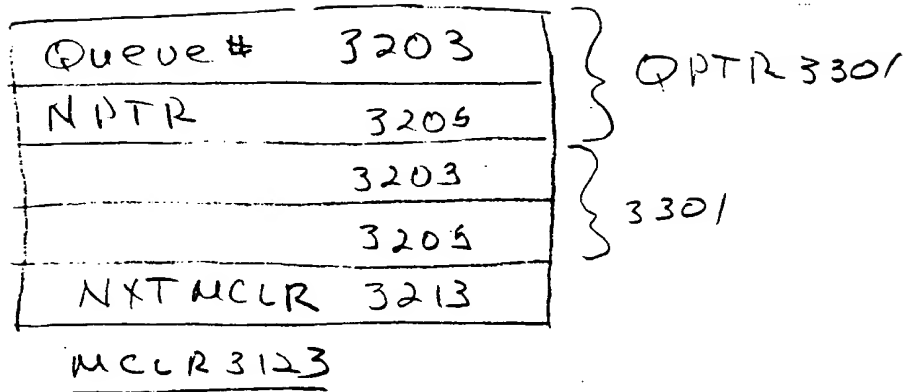
Unicast Queue 215(i)



Unicast Queue 215(j)

Fig. 32

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User #, Queueing Level # 3309

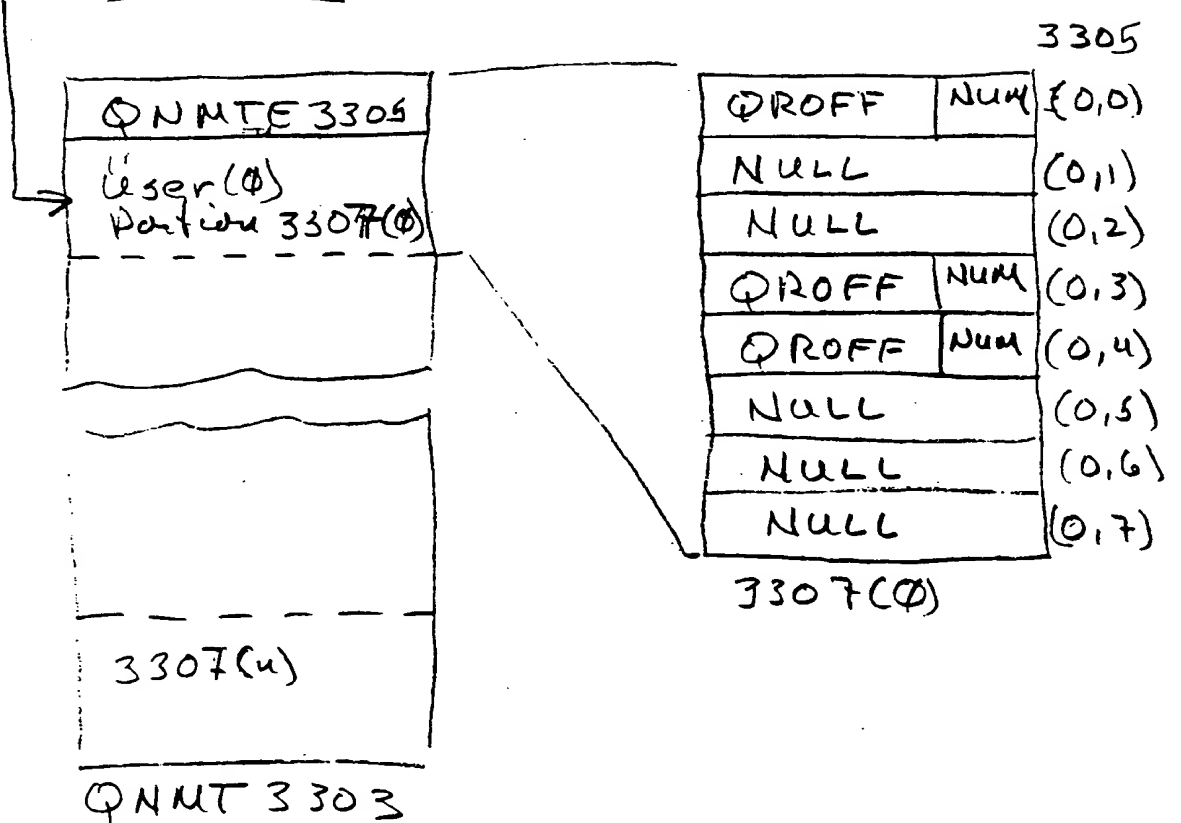


Fig. 33

09674864-0300

09/67/864

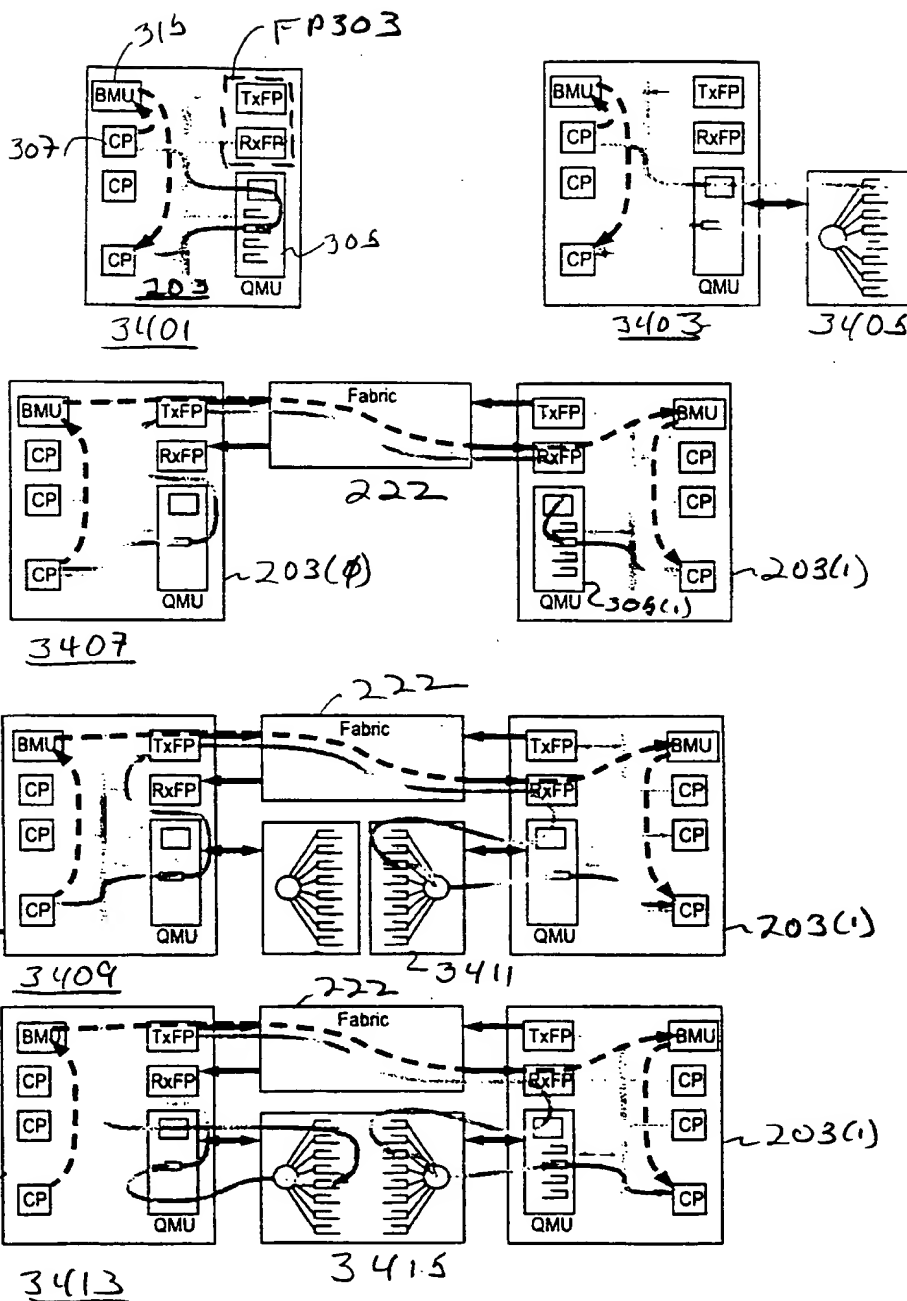
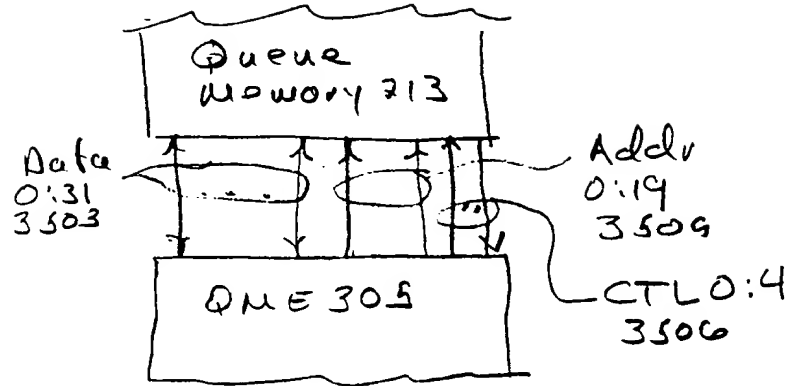
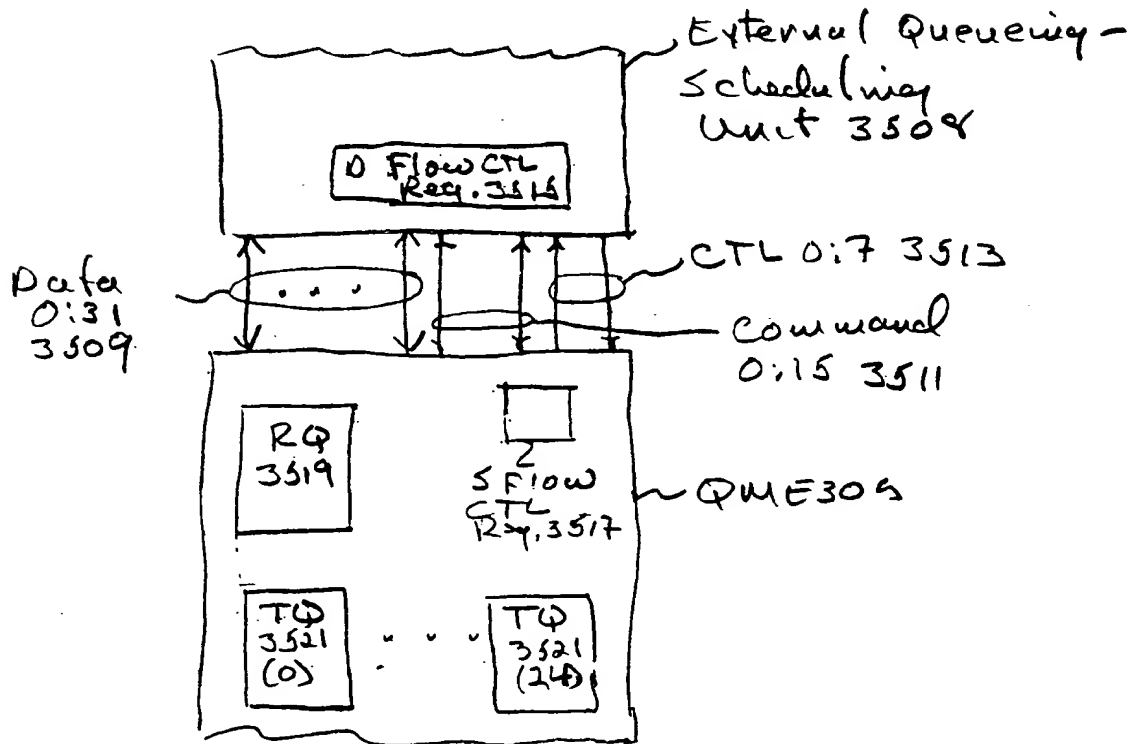


Fig. 34

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Memory External Interface 3501



Scheduler External Interface 3507
35/47

Fig. 35

FIG. 35

09/674864

(Pins 3601
Direction 3603

513	3605	Clk	1	DCP	->	SCHED	
	3607	D_Flow_Ctrl	3	DCP	->	SCHED	
	3609	S_Flow_Ctrl	1	DCP	<-	SCHED	; If = 0, the Scheduler can ; accept at least one descriptor.
	3611	Xfer_Rqst	1	DCP	<-	SCHED	; If = 1, the Scheduler has at ; least one descriptor to transfer.
	3613	Xfer_Ctrl	2	DCP	->	SCHED	
3511		Command Data	16	DCP	<->	SCHED	
		Cmd_Parity	1	DCP	<->	SCHED	
3509		Descript Data	32	DCP	<->	SCHED	
		Data_Parity	1	DCP	<->	SCHED	
		Total	58				

3507

First Command Code 3615

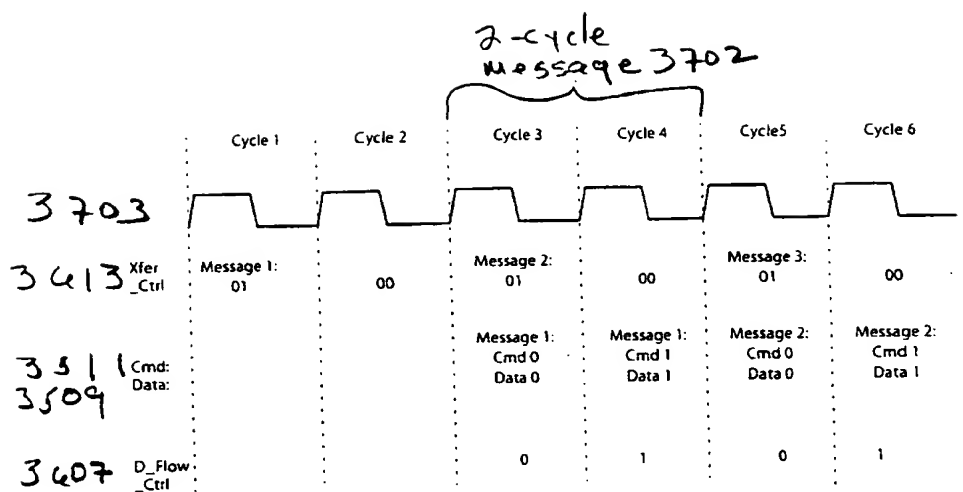
111111
5432109876543210

Destination DCP Processor Number 3617

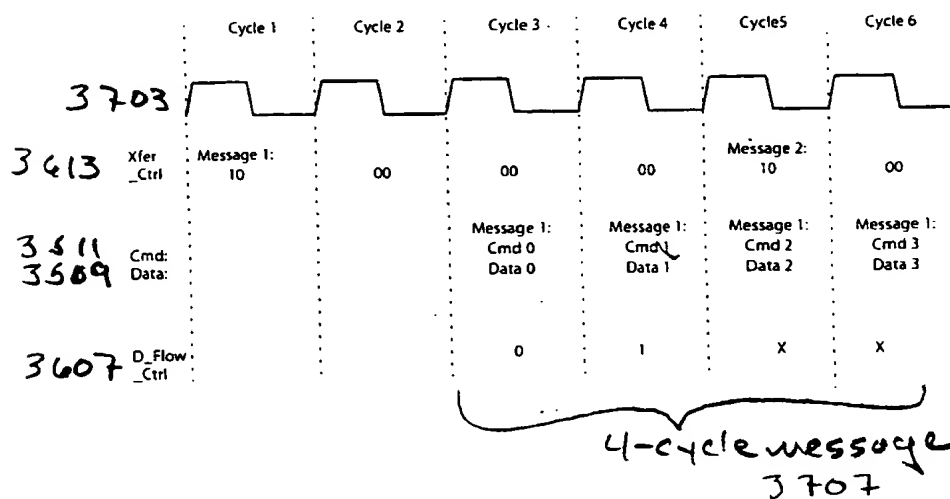
3514

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3701: 2 2-cycle messages



3705: 2 4-cycle messages

Fig. 37

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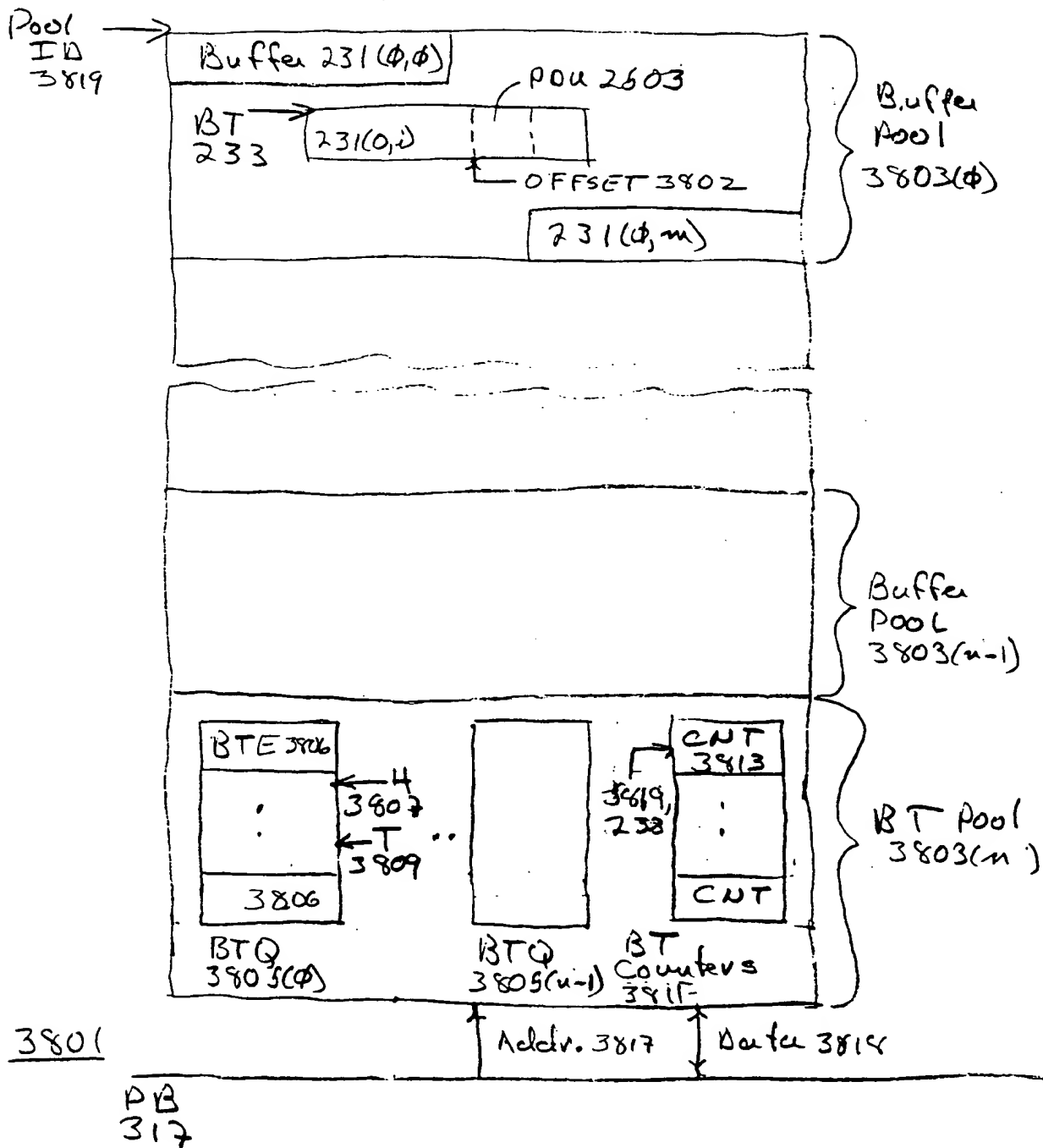
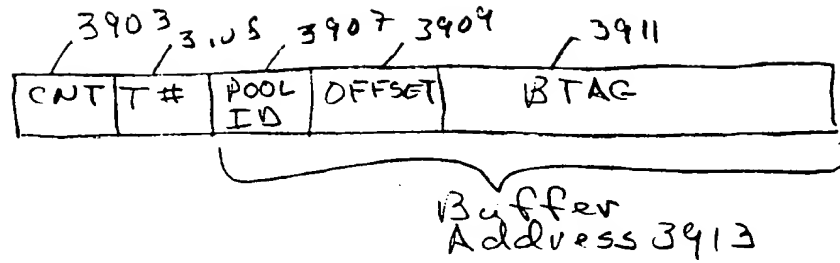


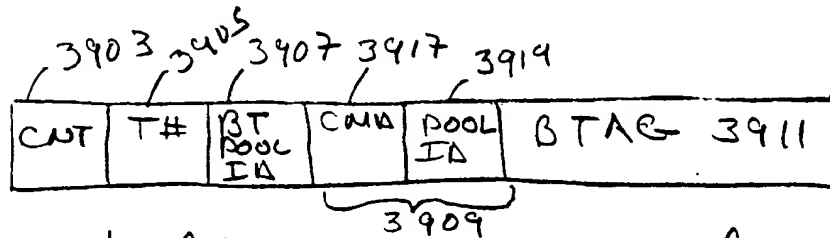
Fig. 38

09/674864



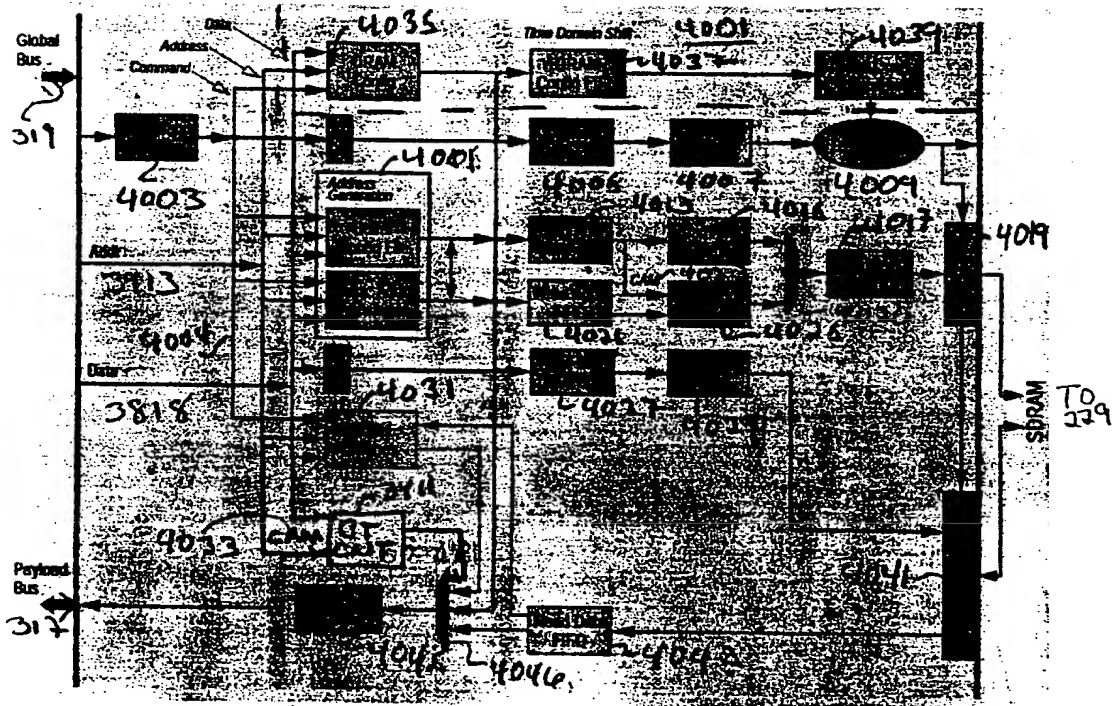
Payload bus

Buffer read/write command 3901



Payload bus BTAG command 3915

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Fig. 410

09674864 033001

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RTOS 4101
BTAG and Buffer Pools 4103

XIP Data Memory 4105

Translation Tables 4107
Packet processor code and Data 4109
Memory Config. Info 4111

229

Fig. 41

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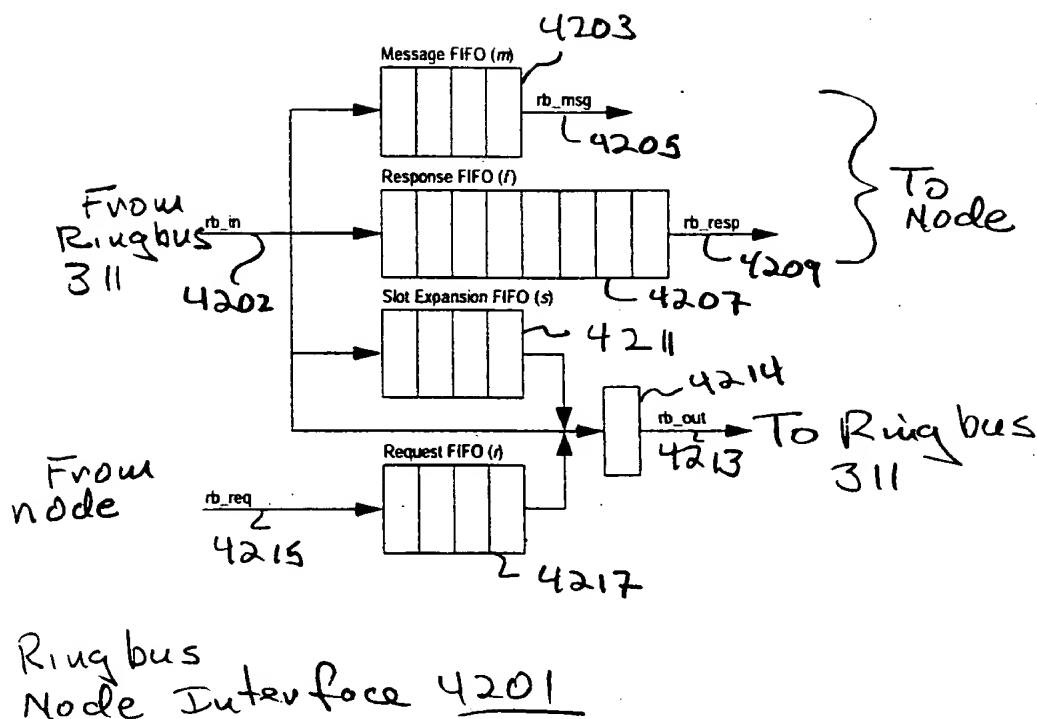
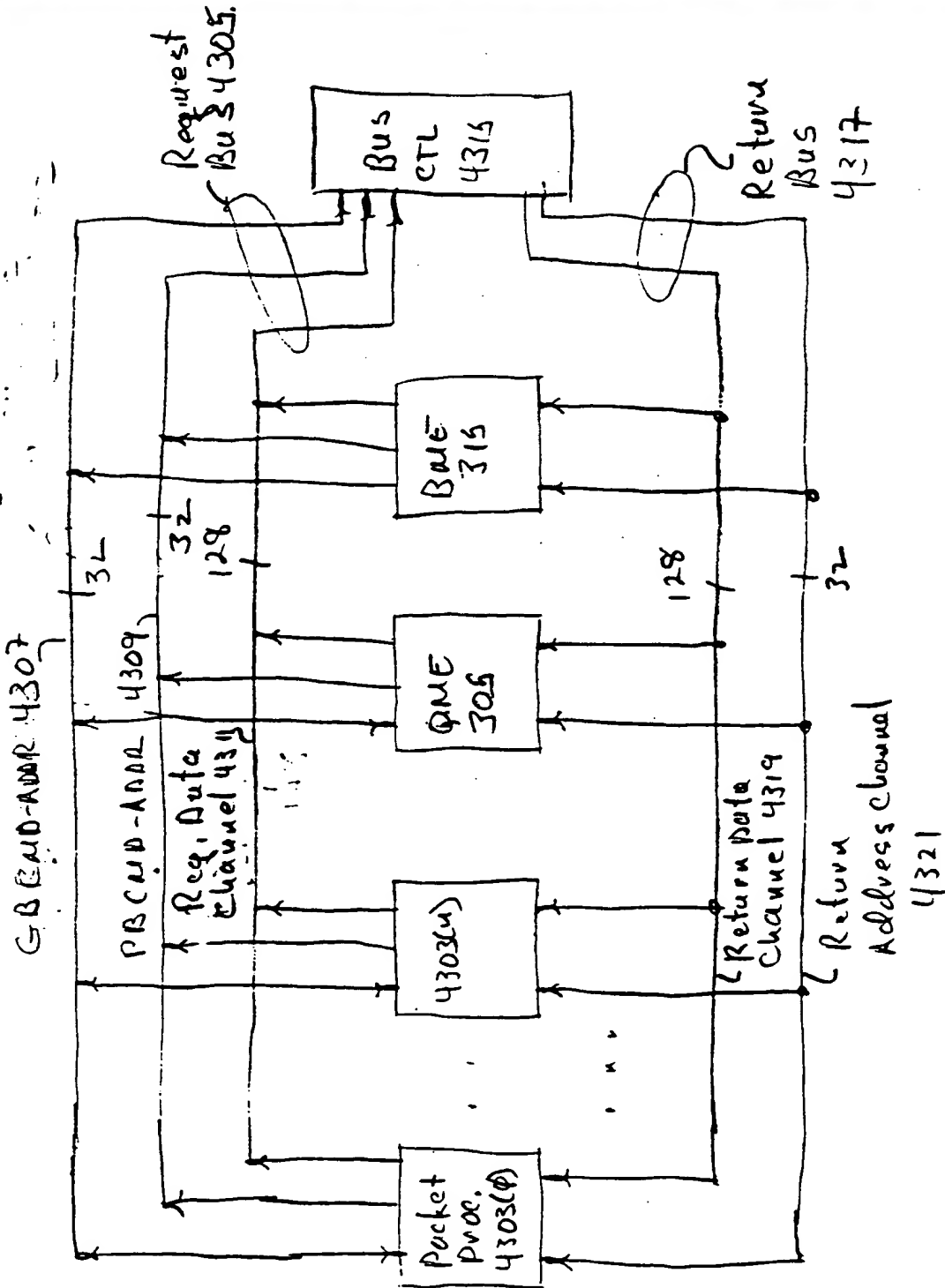


Fig. 42

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FIG. 43

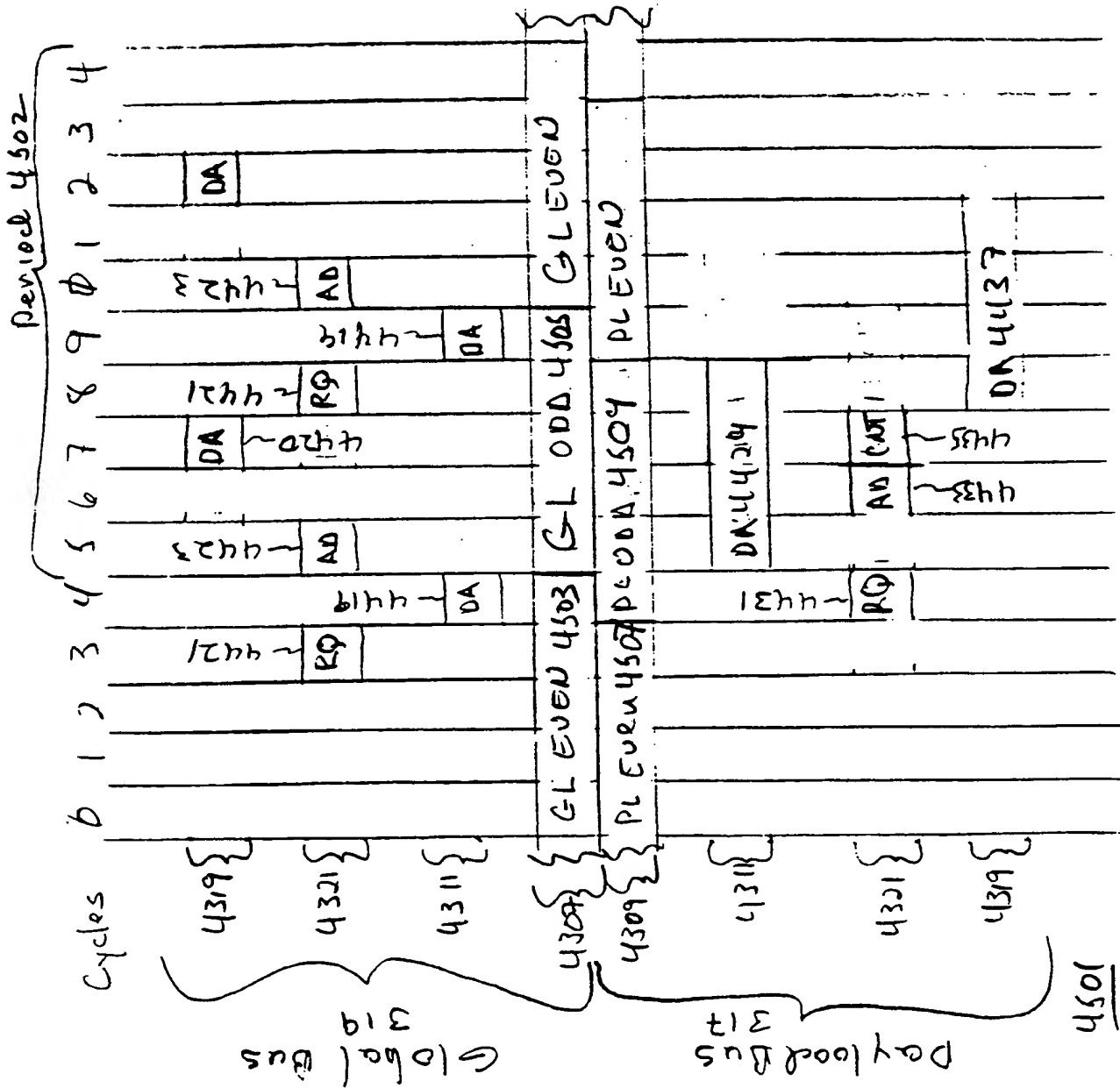


4401

Fig. 44

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TABLE 1984.960



1057
Fig. 45

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4603 4605 4607 4609 4611 4613 4615 4617 4619

Pin	Purpose	RMII	OC-3	DS1	DS3	GMII (Tx)	GMII (Rx)	TBI (Tx)	TBI (Rx)	OC-12
CP0_0	outclk	REF_CLK	RCLK_H	TCLK	TCLK	TCLK	nc	TCLK	nc	TCLK
_1	inclk	CRS_DV	RCLK_L	RCLK	RCLK	CRS	nc		nc	TCLK1
_2	data	TXD[0]	TXD_H	TDATA	TDATA	TXD[0]	nc	TXD[0]	nc	TXD[0]
_3	data	TXD[1]	TXD_L	TxFrame	TxFrame	TXD[1]	nc	TXD[1]	nc	TXD[1]
_4	data	RXD[0]	RXD_H	RDATA	RDATA	TXD[2]	nc	TXD[2]	nc	TXD[2]
_5	data	RXD[1]	RXD_L	RxFrame	RxFrame	TXD[3]	nc	TXD[3]	nc	TXD[3]
_6	data	TX_EN	SIGNAL_DET			TX_EN	nc	TXD[8]	nc	
CP1_0	outclk	REF_CLK	RCLK_H	TCLK	TCLK					
_1	inclk	CRS_DV	RCLK_L	RCLK	RCLK	COL	nc			
_2	data	TXD[0]	TXD_H	TDATA	TDATA	TXD[4]	nc	TXD[4]	nc	TXD[4]
_3	data	TXD[1]	TXD_L	TxFrame	TxFrame	TXD[5]	nc	TXD[5]	nc	TXD[5]
_4	data	RXD[0]	RXD_H	RDATA	RDATA	TXD[6]	nc	TXD[6]	nc	TXD[6]
_5	data	RXD[1]	RXD_L	RxFrame	RxFrame	TXD[7]	nc	TXD[7]	nc	TXD[7]
_6	data	TX_EN	SIGNAL_DET			TX_ER	nc	TXD[9]	nc	
CP2_0	outclk	REF_CLK	RCLK_H	TCLK	TCLK					
_1	inclk	CRS_DV	RCLK_L	RCLK	RCLK	nc	RCLK	nc	RCLK	RCLK
_2	data	TXD[0]	TXD_H	TDATA	TDATA	nc	RXD[0]	nc	RXD[0]	RXD[0]
_3	data	TXD[1]	TXD_L	TxFrame	TxFrame	nc	RXD[1]	nc	RXD[1]	RXD[1]
_4	data	RXD[0]	RXD_H	RDATA	RDATA	nc	RXD[2]	nc	RXD[2]	RXD[2]
_5	data	RXD[1]	RXD_L	RxFrame	RxFrame	nc	RXD[3]	nc	RXD[3]	RXD[3]
_6	data	TX_EN	SIGNAL_DET			nc	RX_DV		RXD[8]	FP
CP3_0	outclk	REF_CLK	RCLK_H	TCLK	TCLK					
_1	inclk	CRS_DV	RCLK_L	RCLK	RCLK			nc	RCLKN	
_2	data	TXD[0]	TXD_H	TDATA	TDATA	nc	RXD[4]	nc	RXD[4]	RXD[4]
_3	data	TXD[1]	TXD_L	TxFrame	TxFrame	nc	RXD[5]	nc	RXD[5]	RXD[5]
_4	data	RXD[0]	RXD_H	RDATA	RDATA	nc	RXD[6]	nc	RXD[6]	RXD[6]
_5	data	RXD[1]	RXD_L	RxFrame	RxFrame	nc	RXD[7]	nc	RXD[7]	RXD[7]
_6	data	TX_EN	SIGNAL_DET			nc	RX_ER	nc	RXD[9]	LOCKDET

Fig. 46

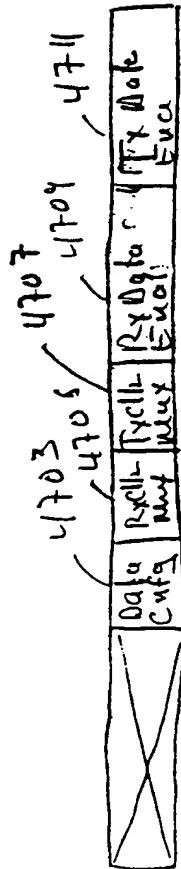
4601

TABLE 19-10

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FIG. 47



4701

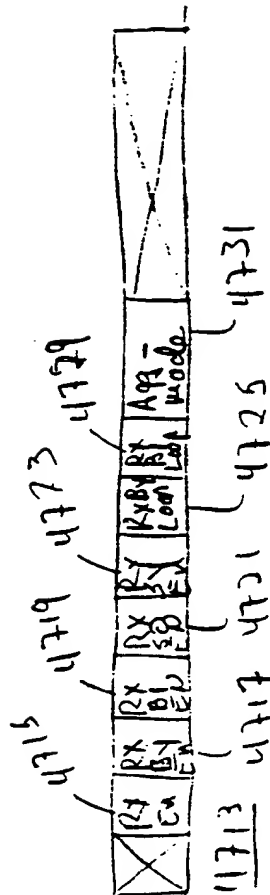


Fig. 47